MODEL 451
Microwave Pulse Counter

EIP Microwave, Inc
2731 North First Street, San Jose, CA 95134
TEL (408) 946-5700
TWX 910-338-0155

Manual Part Number : 5580010 - 02
Printed in U.S.A. - March 1982
CCN : 1004

Printing History

New editions will incorporate all update material since the previous edition. The date on the title page changes when a new edition is published. If minor corrections and updates are incorporated and the manual is reprinted to meet inventory requirements, the date on the title page will not change, but the List of Effective Pages will list that changed information.

FIRST EDITION .....Feb. 1976
SECOND EDITION .....Mar. 1982

List of Effective Pages

This List of Effective Pages gives the most recent date on which the technical material on any given page was altered. If a page is simply rearranged due to a technical change on an adjoining page it will not be listed as a changed page. Within the manual the specific changes are marked with a vertical bar in the margin.

Second Edition .....March 1982

NOTE: THIS SECOND EDITION INCORPORATES ALL REVISIONS UP TO FEBRUARY 1982. THIS EDITION NOW INCLUDES THE OPTION P5, GPIB, THUS ELIMINATING THE NEED TO PROVIDE A SEPARATE MANUAL FOR THAT INFORMATION.

Table of Contents

Table of contents, continued

Table of contents, continued

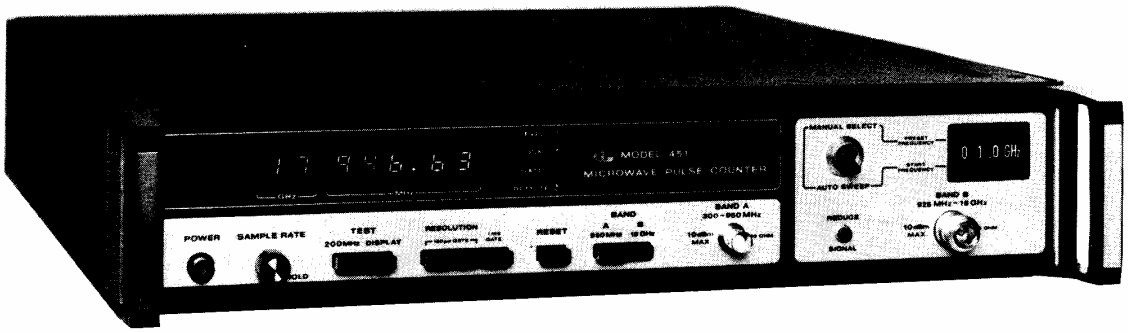
PAGE

Section 9, (Continued)

List of Illustrations

List of Illustrations, continued

Section 1
General Information



DESCRIPTION

The EIP Model 451 Microwave Pulse Counter automatically and directly measures the frequency of pulse modulated microwave signals between 300 MHz and 18 GHz. Pulse widths can be as narrow as 100 n sec., with no maximum width, and 2.5 MHz maximum pulse repetition frequency limits.

The 451 also measures the frequency of CW microwave signals, and carrier signals with FM modulation up to 40 MHz peak-to-peak deviation at 10 MHz modulation rates. No manual switching is required to measure CW or pulsed frequencies. The counter will automatically measure either type of signal. Sensitivity is -10 dBm to 10 GHz; -5 dBm to 18 GHz. A built-in limiter provides overload protection of up to 1 watt peak from 925 MHz to 18 GHz.

All front panel controls except SAMPLE RATE are externally programmable. One input to the counter (Band B) accepts signals over the range of 925 MHz to 18 GHz. Option P2 provides a second input (Band A) to cover the range of 300 MHz to 950 MHz.

The display provides a direct readout of the measured frequency over the entire operating range of the counter, with 10 kHz resolution. The counter also includes automatic suppression of leading zeros, except during a no signal input condition.

The frequency readout of the 451 is displayed in a fixed position format that is sectionalized in GHz and MHz. Gate times are 100 u sec and 1 m sec.

For applications where less resolution is required, pushbutton display blanking (RESOLUTION) is provided to simplify the readout.

To assure trouble free performance, the 451 is completely solid state. For ease of repair and maintenance, the major portion of the counter circuitry is contained on plug-in printed circuit boards or in removeable modules. Special test points allow monitoring of critical functions.

SPECIFICATIONS

GENERAL

Frequency Range Band A Band B	300 MHz to 950 MHz (Option P2) 925 MHz to 18 GHz
Pulse Characteristics Pulse width Pulse repetition freq. Time between pulses	100 nsec min. (measured at 3 dB points) Minimum-50 Hz normal, 0 Hz rear panel selected, Maximum - 2.5 MHz 300 nsec Minimum
Accuracy CW or pulses >100 μsec Pulse <100 μsec	Time base accuracy ±1 count Time base accuracy ± averaging error ± gate error
Averaging error (kHz rms) 100 μs Gate 1 ms Gate	Band A: $\frac{200}{\sqrt{PW-.03}}$; $\frac{60}{\sqrt{PW-.03}}$ Band B: $\frac{100}{\sqrt{PW-.03}}$; $\frac{30}{\sqrt{PW-.03}}$
Gate error (max.)	Band A: $\pm \frac{100\ kHz}{PW-.03}$ Band B: $\pm \frac{40\ kHz}{PW-.03}$ PW = pulse width in μs.
Time Base	Standard: Room Temperature Crystal Option P1: Temperature Compensated Crystal (TCXO)
Crystal frequency	10 MHz
Stability Aging rate	$< \lvert 3 \times 10^{-7} \rvert$ /mon.
Temperature (0-50°C)	Standard: $< \lvert 3 \times 10^{-5} \rvert$ Option P1: $< \lvert 2 \times 10^{-6} \rvert$
Line voltage	±10% change produces frequency shift $< \lvert 1 \times 10^{-7} \rvert$
Warm up time	None required
Sensitivity Band A (Opt. P2) Band B	300 to 950 MHz -10 dBm peak 925 MHz to 10 GHz -10 dBm peak 10 GHz to 18 GHz -5 dBm peak
FM Tolerance Band B (minimum)	CW: 40 MHz p-p deviation for mod. rates DC-10 MHz. PULSE (w/o Input Inhibit): 20 MHz max. freq. shift across pulse. FREQUENCY PROFILE (using Input Inhibit): 20 MHz max. freq. shift during input inhibit pulse.

GENERAL, continued

Maximum Input Level (peak)	Operating	Burnout Level
Band A 300 to 950 MHz (Opt. P2)	+10 dBm	+27 dBm
Band B 925 MHz to 18 GHz	+10 dBm	+30 dBm
	Band A (Opt. P2)	Band B
Input Impedance	50 Ω nom.	50 Ω nom.
Connector	BNC	Type N precision
Measurement Speed (Band B Only) Acquisition Time PRF >100 Hz PRF <100 Hz	100 msec + 50 msec/GHz 100 msec + $\frac{5}{PRF}$ sec/GHz	
Reading Time Band B (sec)	Band A	Band B
100 μs Gate	$\frac{400}{(PW-.03)(PRF)}$	$\frac{100}{(PW-.03)(PRF)}$
1 ms Gate	$\frac{4000}{(PW-.03)(PRF)}$	$\frac{1000}{(PW-.03)(PRF)}$
	PW = pulse width (μsec) PRF = pulse repetition frequency (Hz)	
Display	7 digit LED with fixed decimal point. Leading zero suppression.	
Resolution	10 kHz, 100 kHz, 1 MHz	
Power	100/120/220/240 VAC ±10%, 50-60 Hz, 100 watts nominal.	
Operating Temperature	0 to 50°C	
Weight	Net 30 lbs. Shipping 35 lbs.	
Dimensions	3.5" high and 16.75" wide and 19" deep	
Accessories Furnished	8 foot power cord and instruction manual	
Accessories Available	Model 400 Delay Generator. Carrying Case. P/N 5700001 Rack Mtg. Kit. P/N 2010008	

SPECIFICATIONS, continued

FRONT PANEL

Controls	
Sample Rate/Hold	Varies display reading time from 0.1 sec/reading to 10 sec/reading. "Hold" displays last reading.
Test-200 MHz	Displays 200 MHz internal test frequency.
Display Test	Tests all LED numeral segments.
Resolution	(1 MHz, 100 kHz, 10 kHz): Sets display resolution.
1 ms Gate	Selects 1 ms gate.
Band Select (A or B)	Switch selects either Band A (Opt. P2) or Band B input.
Auto/Manual (Band B)	
Auto Mode	Band B searches upward for input signal beginning 105 MHz above preset number.
Manual Mode	Inhibits search. Signal must lie between 105 MHz and 325 MHz above preset number.
Thumbwheel Switch (Band B)	
Auto Mode	Sets start point of frequency sweep (105 MHz above preset number.)
Manual Mode	Sets operating frequency range (105 MHz to 325 MHz above preset number.)
Indicators	
Level	Indicates sufficient input level.
Lock	Indicates signal acquired.
Gate	Indicates measurement in process.
Remote	Indicates Remote Programming (Option P4 or P5) active.
Reduce Signal (Band B)	Indicates signal level above optimum operating range.
Connectors	
Band A input	Type BNC female - 300 to 950 MHz (Option P2)
Band B input	Type N precision female - 925 MHz to 18 GHz

REAR PANEL

Controls	
Power input	Power module containing AC connector, fuse, and voltage control for 100, 120, 220, or 240 VAC.
Storage (On/Off)	Normally on. In off position, display updates continuously during measurement cycle.
Min. PRF = (50 Hz/0)	Normally in 50 Hz position. In 0 position, allows measurements of very low PRF signal.
Connectors	
10 MHz reference output	1 V peak-to-peak min. into 50 Ω
Gate Output	-0.5v min. into 50 Ω corresponding to counter gate.
Signal Threshold Output	-0.5v min. into 50 Ω corresponding to signal exceeding threshold.
Inhibit Input	ECL high (-0.9v) inhibits. ECL low (-1.7v) enables. From 50 Ω source, 0 volts will inhibit, -1v will enable. Input impedance: 50 Ω to -2 volts.

OPTIONS

P1	TCXO - temperature compensated crystal oscillator
P2	Band A: 300 - 950 MHz
P3	Rear panel inputs: Band A and B
P4	BCD output/remote programming Remote programming: provides rear panel programming of all front panel controls except SAMPLE RATE. Requires ground contact closure; one control line per function (T^2L and DTL compatible). Digital output: 7 data digits in parallel form. 1-2-4-8 "1" state positive.
P5	GPIB: System interface per IEEE STD 488-1975.

Section 2
Installation

UNPACKING

The 451 counter arrives ready for operation. Carefully inspect the shipping carton before opening for any evidence of visible or concealed damage. If any seems apparent, ask that the shipper's agent be present when the counter is unpacked.

Remove the packing carton and supports, being careful not to scar or damage the counter. Make a complete visual inspection of the counter, checking for any damage or missing components. Check that all switches and controls operate mechanically. Report any damage to EIP immediately.

INSTALLATION

There are no special installation instructions for the 451. The unit is a self-contained bench or rack mounted instrument, which only requires connection to a standard, single-phase, 100/120 or 220/240 volt, 50-60 Hz power line for operation.

CAUTION

Check current rating of counter fuse and voltage range PC board in power module (on rear panel of counter) before applying power to the counter. Module PC board should show the correct nominal line voltage when installed in the module.

INCOMING OPERATIONAL CHECK

The following procedure outlines an operational check of the counter which may be conducted without special tools, signal generators, or test equipment. In the 200 MHz test function the internal Time Base Clock is used as the input signal to the Direct Counter, therefore it cannot check the operation of the Band A Prescaler or the Band B Converter.

1. Turn counter POWER switch off. Check fuse rating and card in power module.

2. Connect counter power cord to the voltage source. The ground terminal on the power cord plug should connect to a reliable earth ground.

3. Press POWER switch (on front panel) to turn counter on. The counter display should light, and the internal cooling fan should operate.

4. Partially depress either of the two RESOLUTION switches and release it, so neither switch remains in the depressed position. All digits in the display should indicate "0" (zero).

5. Depress the front panel 200 MHz TEST switch. The display should indicate "200.00".

6. Blank the 10 kHz digit by pressing the right hand RESOLUTION switch.

7. Depress the 200 MHz TEST button again. The display should indicate "200.0".

8. Test both RESOLUTION switches. Note that the digit immediately above the switch, and any digit to the right will be blanked.

9. Unblank all display digits (see "4" above).

10. With no input signal, the entire display should show all zeros in both positions of the BAND switch.

11. Depress the DISPLAY TEST switch. All display digits should show "8" (all segments of each digit lighted).

This completes the counter operational check.

INSTRUMENT IDENTIFICATION

The 451 is identified by two number sets: the model and configuration control number (e.g. 451-CCN 1004), and a specific Serial Number (e.g. 12345). Both sets of numbers should be mentioned in any correspondence or parts orders relating to the counter.

Section 3
Operation

INTRODUCTION

The 451 has three principle modes of operation: automatic, manual, and externally enabled. This section will describe each of these modes, and will provide information on timing considerations and instrument accuracy.

WARNING

DO NOT APPLY A SIGNAL EXCEEDING THE MAXIMUM INPUT SPECIFICATION TO ANY INPUT. EXTENSIVE DAMAGE, NOT COVERED BY WARRANTY, WILL OCCUR EVEN IF THE COUNTER IS TURNED OFF, OR APPEARS TO BE INOPERATIVE.

AUTOMATIC MODE

In this mode either CW or pulse signals can be measured. Connect the input frequency to the appropriate input connector (Band A, option P2, for frequencies between 300 MHz and 950 MHz; Band B for frequencies between 925 MHz and 18 GHz). If the input signal is sufficient for counting, the LEVEL indicator will light. If the proper band and input have been selected, the LOCK indicator will light. In Band B, if the input signal is too high, the REDUCE SIGNAL indicator will light. Measurements will be made at a rate that is determined by the SAMPLE RATE control.

In Band B, acquisition speed may be improved by presetting the start frequency via the thumbwheel switch. The minimum frequency which can be acquired will then be 105 MHz above the switch setting.

CAUTION

An erroneous reading may result if an applied signal is less than 105 MHz above the switch setting.

MANUAL MODE

The manual mode is possible in Band B only. It is done by setting the MANUAL SELECT/AUTO SWEEP switch to the manual select position, and the thumbwheel switch to the proper frequency. In manual mode the operating frequency range is from 105 MHz to 325 MHz above the switch setting. Since no sweep is required, the acquisition time is eliminated.

CAUTION

Application of signals not between 105 and 325 MHz more than the switch setting may result in reading errors.

EXTERNALLY ENABLED MODE

The use of the rear panel INPUT INHIBIT makes possible a class of measurements – measurements made at a specified point in time on a signal whose frequency is some repetitive function of time. When a high level is applied, the 451 is inhibited from making a measurement. Thus a signal at the INPUT INHIBIT can be used as an enable signal to make a measurement at a desired time. The width of the enable signal determines the duration of the measurement – typically 30 nanoseconds less than the applied pulse.

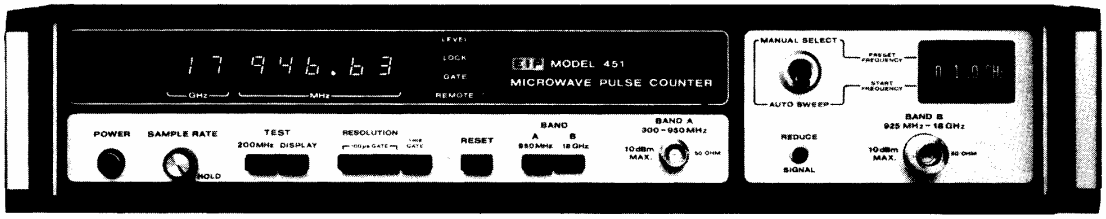


Figure 3-1. Front View, 451 Microwave Pulse Counter

FRONT PANEL CONTROLS

POWER On/Off SWITCH

Turns counter power on and off.

SAMPLE RATE/HOLD CONTROL

Continuously variable control for one-tenth to ten seconds per reading. (Required Gate time is added to sample time). HOLD position retains reading until manually reset.

200 MHz TEST SWITCH

Provides check of internal counter circuits. Display should indicate "200.00" MHz.

DISPLAY TEST SWITCH

Displays "88 888.88" to test all LED segments.

RESOLUTION (100 μs GATE) SWITCHES

Provide blanking of either one or two least significant digits for resolution of 10 kHz, 100 kHz, or 1 MHz, with 100 microsecond gate time.

1 ms GATE SWITCH

Provides 10 kHz resolution with 1 millisecond gate time for reduced pulse averaging error.

RESET SWITCH

Manually overrides the SAMPLE RATE/HOLD control, resets display to zero, and initiates a new reading.

BAND SELECT SWITCHES

Select desired operating band – either BAND A (Option P2 - 300 MHz to 950 MHz), or BAND B (925 MHz to 18 GHz).

BAND A CONNECTOR

BNC female connector for Band A input (Option P2).

VISUAL DISPLAY

The 7-digit LED (light-emitting-diode) display provides a direct numerical readout of the input frequency. The display is sectionalized into GHz and MHz ranges.

LEVEL INDICATOR

When lit, indicates that input signal is of sufficient level for counting. Blinking light indicates that PRF (pulse repetition frequency) is too low.

LOCK INDICATOR

When lit, indicates that input signal has been acquired.

GATE Indicator

Indicates that counter is in measurement portion of its cycle.

REMOTE INDICATOR

Used with Option P4 (BCD/Remote Programming). When lit, indicates that Remote Enable has been activated, and that all front panel controls except SAMPLE RATE are disabled. Also used with Option P5 (GPIB).

MANUAL SELECT/AUTO SWEEP SWITCH

Selects manual or automatic operation for Band B.

PRESET/START FREQUENCY THUMBWHEEL SWITCH

In the MANUAL mode, the switch sets the operating frequency range. The signal must lie between 105 MHz to 325 MHz above switch setting. In the AUTOMATIC mode, the switch sets the start of the search range. Input frequency must be at least 105 MHz above switch setting.

REDUCE SIGNAL INDICATOR

Indicates excessive signal input to Band B. **WARNING:** Signals in excess of rated specifications may cause extensive damage NOT covered by the warranty.

BAND B CONNECTOR

Type N precision connector for Band B operation.

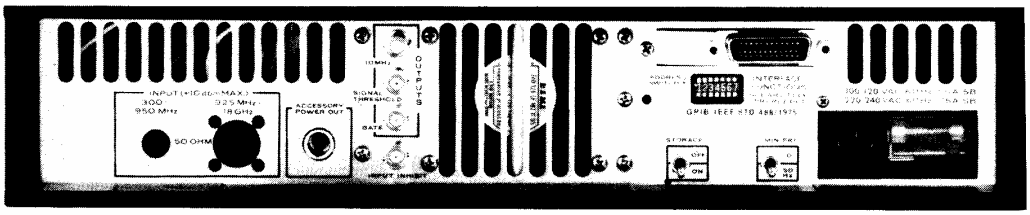


Figure 3-2. Rear Panel, 451 Microwave Pulse Counter

REAR PANEL CONTROLS

REAR PANEL INPUTS

(Option P3) allows modification of counter for rear panel inputs.

ACCESSORY POWER OUT CONNECTOR

Provides power for 451 Pulse Counter accessories.

10 MHz OUTPUT CONNECTOR

Output of internal 10 MHz clock, 1 Vp-p minimum into 50 ohms.

SIGNAL THRESHOLD

Pulse output representing signal threshold level of input pulse. Typically occurs 20 nanoseconds after input pulse, and is used for frequency profile measurements.

GATE OUTPUT CONNECTOR

Provides Gate pulse representing actual time at which measurement is being made. Used in frequency profile measurement.

INPUT INHIBIT CONNECTOR

External pulse input for frequency profile measurements.

REMOTE INPUT/OUTPUT CONNECTOR

(Option P4) Connector for BCD/Remote Programming.

GPIB INPUT/OUTPUT CONNECTOR

(Option P5) For connection to General Purpose Interface Bus (IEEE STD 488-1975).

STORAGE SWITCH

Normally ON. In the OFF position, display updates continuously during measurement cycle.

MIN PRF SWITCH

Normally in 50 Hz position. In 0 position, allows measurement of very low PRF signal. NOTE: Reading will not automatically reset when signal is removed.

AC POWER MODULE

Contains AC power line receptable, fuse, and PC board for voltage selection.

DISPLAY ADJUSTMENT

Apparent brightness of the light-emitting-diode (LED) numerical display may be varied by adjustment of potentiometer A102R35. (R35 is located near the top front of PC Board A102, and is accessible by removing the top cover of the counter.) Adjust R35 clockwise to increase display brightness, or counter-clockwise to decrease the brightness.

INPUT INHIBIT

The INPUT INHIBIT on the 451 is designed to be compatible with either a 50 ohm impedance pulse generator, or emitter-coupled-logic (ECL) devices. An internal termination of 50 ohms returned to -2 volts makes this dual compatibility possible. An ECL high level signal (-0.8 to -1.1 V) will inhibit measurement. ECL devices are designed to drive 50 ohm lines without reflections when the lines are terminated with 50 ohms returned to -2 V. The direct compatibility with a 50 ohm pulse generator results from the fact that zero volts from a 50 ohm source will produce -1V at the INPUT INHIBIT (inhibiting the 451), while a -1 V signal into 50 ohms will produce 1.5 V at the INPUT INHIBIT thus enabling the 451.

PULSE MEASUREMENT

Automatic pulse measurements can determine the average frequency of a pulse. In some cases however, additional information may be necessary. For example, a pulsed magnetron may exhibit substantial frequency shift near the leading and trailing edges of the pulse, or a pulsed Gunn diode oscillator may exhibit frequency shift during a pulse due to peak power thermal effects. Measurements of these characteristics are easily made with only the 451 and a delaying pulse generator (see Figure 3-3). The SIGNAL

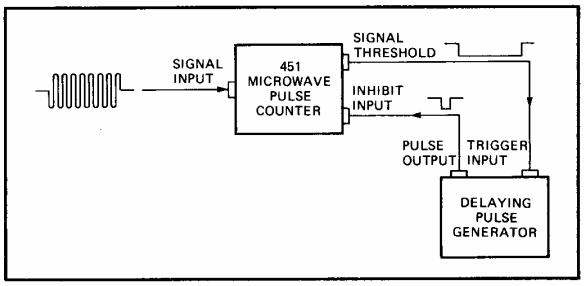


Figure 3-3. Pulse Profile Measurement Test Set-Up.

THRESHOLD output of the 451 is used to trigger the pulse generator. The generator's output pulse is used as an enable input to the 451. As the pulse delay is varied, the measurement window can be "walked" through the pulse. A plot of frequency-versus-delay gives the frequency-versus-time profile of the pulse directly, as shown in Figure 3-4. The width of the measurement window is determined by the width of the pulse generator output. Measurement windows of 50 nsec or less can be used, although wider windows yield higher accuracy.

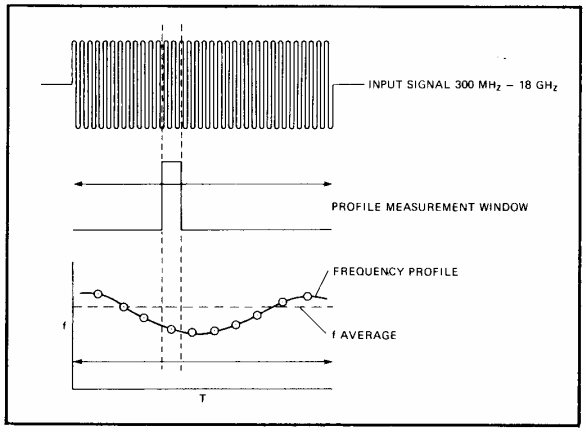


Figure 3-4. Pulse Profile Measurement

TIME VARYING SIGNALS

Many complex signals are not pulses at all, but simply continuous signals that have frequency variations repetitively with time. One example is the measurement of the response of a VCO. A square wave applied to the tuning voltage will produce a response curve of frequency-versus-time, allowing measurement of linearity and amplitude for frequency modulated radar altimeter signals. Figure 3-5 shows a test set-up designed to make measurements on time varying signals. It is similar to the pulse profile test set-up, except that there is always a signal present, and a trigger must be obtained from the modulating source. This will trigger the pulse generator which controls the measurement.

MULTIPLE SIGNAL MEASUREMENTS

Another type of measurement is that of a repetitive sequence of pulses that differ in frequency. In this case, it is desirable to measure the frequency of each pulse in the sequence separately. The same test set-up as shown in Figure 3-5 is required, with the trigger pulse synchronous with the sequence. In this measurement the INPUT INHIBIT is used to discriminate between pulses. The enabling pulse can be slightly wider than the pulse to be measured. By shifting the delay time of the enabling pulse, each input pulse of the sequence can be separately measured.

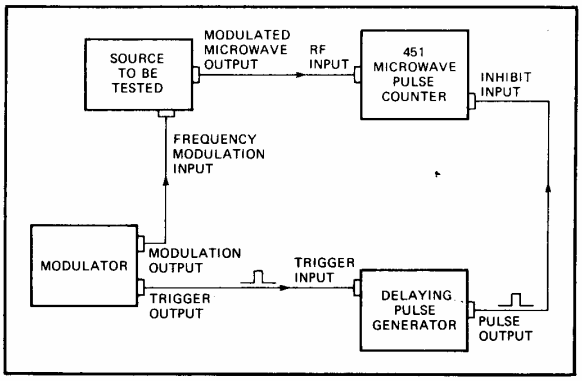


Figure 3-5. Time Varying Signal Measurement Test Set-up

TIMING CONSIDERATIONS

The internal timing usually should be of no concern to the user. However, in applications where a few nanoseconds are significant, some details of internal operation are important. These involve two areas. One area is the measurement window width, and the other is the internal timing delays.

MEASUREMENT WINDOW WIDTH

The measurement window is the period during which the gate is actually open to enable the counting of a signal. This gate width will typically be 30 nanoseconds narrower than the pulse applied to the INPUT INHIBIT. The width of the gate is always an integral number of clock periods (5 nsec.). For applications where the measurement window needs to be known to an accuracy better than 20 nsec., it is recommended that the gate output on the rear panel be observed on a high speed oscilloscope. The desired gate width may be set by varying the INPUT INHIBIT pulse width. For accurate pulse representation, the oscilloscope input should be terminated in a 50 ohm load.

INTERNAL TIMING DELAYS

When it is necessary to measure the signal frequency at a precise point in time, the internal delays of the measuring instrument can be significant. In the 451 the total delay between the time a signal is applied to an input connector, and the time it is available to be counted, is nominally 60 nsec. The signal threshold output, on the rear panel, typically occurs 20 nsec. after the signal is applied. The gate signal, at the rear panel, occurs at the measurement time with virtually no delay. In other words, when absolute time positioning of a signal is required, it is necessary to consider that the gate signal (representing the measurement period) is actually making a measurement of the signal which appeared at the input connector 60 nsec earlier. If the signal threshold output is used as an indication of input signal then it occurs 40 nsec prior to measurement. Figure 3-6 shows the relative timing of these signals for a pulsed input signal. Timing however, is not a function of input signal characteristics.

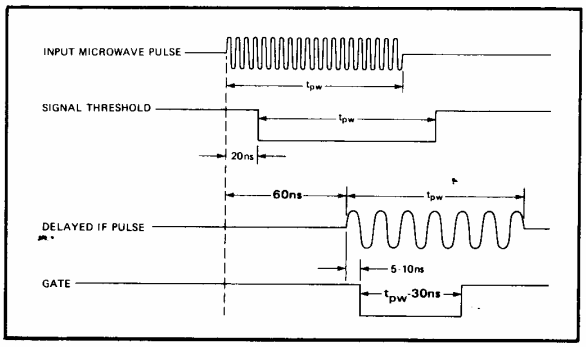


Figure 3-6. Internal Timing Delays

ACCURACY

In a CW frequency counter, measurement accuracy is generally specified as "time base accuracy ± 1 count". This means that the frequency measurement is in error by the same percentage as the time base reference oscillator. The maximum error in the time base is the sum of various possible errors, such as aging rate, temperature, etc.

The second type of error: ± 1 count, is derived from the relative timing of gate and signal. Simply stated, if an event occurs every 400 ms (F = 2.5 Hz), a counter could measure either 2 or 3 events in a one second interval.

There is a third possible source of error in a CW counter: gate error. A gate is supposed to represent a precise number of reference oscillator cycles. Due primarily to differences in the rise and fall times of various circuits, the actual gate will usually be a fixed amount wider or narrower than desired. If this error is less than one period of the maximum input frequency, no counter error will occur. Thus a 300 MHz counter needs a gate accurate to about 3 nanoseconds.

Each of these three sources of error can contribute to the overall error in pulse frequency measurements. In fact for narrow pulses, the second and third sources of error which are usually ignored in a CW counter, become the dominate sources of error in a pulse counter.

TIME BASE ERRORS

A frequency error in the time base references oscillator, results in a proportional frequency measurement error. Two main sources of time base error are: aging rate, and temperature. Aging rates of $< | 3 \times 10^{-7} |$/ month, and temperature stability of $< | 3 \times 10^{-5} |$ over the range of 0 to +50° C, are standard on the 451. An optional temperature compensated crystal oscillator (TCXO) reduces temperature instability to $< | 2 \times 10^{-6} |$. By calibration against a frequency standard, this error can be made less than one count, and thus becomes insignificant.

AVERAGING ERROR

In order to obtain high resolution, the frequency of a number of measurements is averaged. Each individual measurement has a ± 1 count uncertainty as previously noted. If N measurements are made, then an uncertainty of ± N counts is possible, but very unlikely. The resultant averaged measurement will follow the rules of statistics, in that successive measurements will vary randomly to a certain degree. In fact, most of the readings (63%) will fall between $\pm \sqrt{N}$ counts — this is called the RMS averaging error. N is the number of gates required to accumulate 100 μs (or 1 ms) of gate time. The gate is typically 30 ns narrower than the input pulse, so the RMS averaging error is:

$$\text{Averaging Error (RMS)} = \frac{100 \text{ (or 30) kHz}}{\sqrt{PW - .03}} \ ^{*}$$

PW = Pulse width in μs. * 30 kHz with 1 ms gate, 200 (or 60) kHz for Band A. NOTE: Since Band A gate times are expanded by 4, $\sqrt{N}$ increases by 2.

GATE ERROR

When narrow pulses are counted, the gate is opened many times in order to obtain a high resolution measurement. Each time the gate opens and closes, there will be a small but finite error. The total error is proportional to the number of times the gate is cycled during a measurement, and is thus inversely proportional to the gate width. This error is also related to both temperature and input frequency. In the 451, the worst case error including all variables, is specified as:

$$\text{Max Gate Error} = \frac{\pm 40 \text{ kHz}}{PW - .03}$$

where PW = pulse width in microseconds (± 100 kHz for Band A).

Unlike averaging error which is random, gate error is systematic, and is not reduced by frequency averaging.

TECHNIQUES FOR IMPROVING ACCURACY

In most cases, specified accuracy of the 451 will be more than sufficient to meet measurement requirements. If greater accuracy is required, all three sources of error can be minimized by a combination of error calibration and long term averaging. It is recommended that if very high accuracy is required, the counter include Options P1 (TCXO) and P4 (BCD Output/Remote Programming) or P5 (GPIB).

TIME BASE CALIBRATION

A frequency error in the time base oscillator results in the same percentage error in the frequency reading for either CW or pulsed signals. By directly measuring the 10 MHz time base frequency at the 10 MHz OUTPUT connector using a standard of known accuracy, this error can be determined and corrected. As an example, suppose the measured time base output is 10,0001 MHz, The time base is thus 1×10^{-6} high in frequency, and all reading will be 1×10^{-6} low in frequency — a reading at 10 GHz will be 10 kHz low. Instead of correcting the reading for this error, a better technique is to set the time base oscillator precisely on frequency. The advantage of a 451 equipped with a TCXO is improved settability and temperature stability.

LONG TERM AVERAGING

Averaging error, as noted previously, is simply the result of a random statistical process. As in all such processes, taking a larger number of samples reduces the averaging error. On 451's equipped with BCD Output Option P4 or Option P5, a test set-up as shown in Figure 3-7 allows the random averaging error to be virtually eliminated. The DAC takes the three least significant digits and produces an analog voltage which is plotted on a strip chart recorder. The average value of the output can be easily obtained from the strip chart.

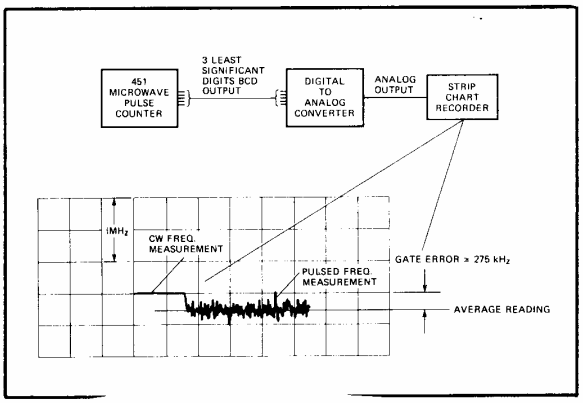


Figure 3-7. Calibration Test Set-Up (Averaging/Gate Error)

GATE ERROR

Gate error at any given frequency and pulse width can be virtually eliminated. This is accomplished by simulating a pulsed input and determining the gate error. This calibration factor can then be added to, or subtracted from, the indicated measurement to obtain the correct frequency. First, determine the gate error using a CW source at approximately the same frequency (within 25 MHz) as the indicated measurement. A pulsed input is then simulated by applying an ENABLE signal - of the same width as the pulse to be measured - to the INPUT INHIBIT connector. Gate error is the difference in reading between the pulsed and non-pulsed measurement of the same CW signal. This procedure provides the true gate error, and avoids error associated with any possible pulling of the signal source. The DAC and strip chart recorder shown in Figure 3-7 can be used to determine the error to a resolution of a few kHz. The result of a typical strip chart is also shown. It should be noted that gate error can be calibrated out of the system for a given pulse width and frequency. However, this calibration procedure will result in additional error for any other pulse width or frequency.

Section 4
Theory of Operation

GENERAL

The 451 Counter automatically measures and displays the frequency of a CW or pulsed signal in the range of 925 MHz to 18 GHz (Band B). An optional Prescaler (Option P2) extends this range downward to 300 MHz (Band A). In addition to fully automatic measurements, it is possible to utilize the 451 with accessory equipment to make dynamic frequency measurements. The frequency of any repetitive signal can thus be measured at any point in time. Measurement windows as narrow as 20 nanoseconds are achievable.

Measurements in Band B (925 MHz - 18 GHz) are achieved by heterodyning the input signal with a known harmonic of 200 MHz. The resulting difference frequency is then processed by a 350 MHz Direct Counter. The counter gate is enabled by the input itself in a manner such that the gate is open only when a signal is present.

In the Direct Counter, obtainable resolution is inversely proportional to the measurement time. For example: A 1 microsecond gate time will yield 1 MHz resolution. To achieve 10 kHz resolution, the 451 automatically averages as many input pulses as necessary to obtain a total gate interval of 100 μs (or 1 ms). The required number of pulses is thus a function of the input pulse width.

In the optional Band A (300MHz - 950 MHz), the input frequency is divided by four. The divided frequency is then counted in the Direct Counter for a 400 μs (or 4 ms) period to obtain a readout with 10 kHz resolution. As in Band B, gating is controlled by the input signal.

The system operation is best described by separating the instrument into its two main functional blocks: the Microwave Converter, and the Direct Counter.

Figure 4-1 shows a simplified block diagram of the entire 451. Figure 4-2 shows a more complete block diagram of the Microwave Converter section, while Figure 4-3 diagrams the Direct Counter. Detailed circuit descriptions of all PC boards are given in Section 8.

MICROWAVE CONVERTER

The Microwave Converter is a self-contained assembly which performs the function of translating the input microwave frequency downward into the range of 105 to 325 MHz. This translation is accomplished by mixing the incoming signal with a known reference frequency and then amplifying the difference. The input frequency is determined by counting this difference frequency and adding it to the known reference frequency (see Figure 4-2).

The reference frequency is an integral harmonic of 200 MHz, generated within the YIG Comb Generator (A207). This unit is an integrated assembly containing a harmonic (or comb) generator, and a two-stage YIG filter. The comb generator converts the 200 MHz sine wave input into a train of narrow pulses containing all the harmonics of 200 MHz up to 18 GHz, while the YIG filter selects the desired harmonic. Tuning of the YIG filter is accomplished by varying the current through a pair of coils, which in turn, varies a magnetic field within the structure. (A more comprehensive description of the operation of a YIG-tuned device is given later in this section.)

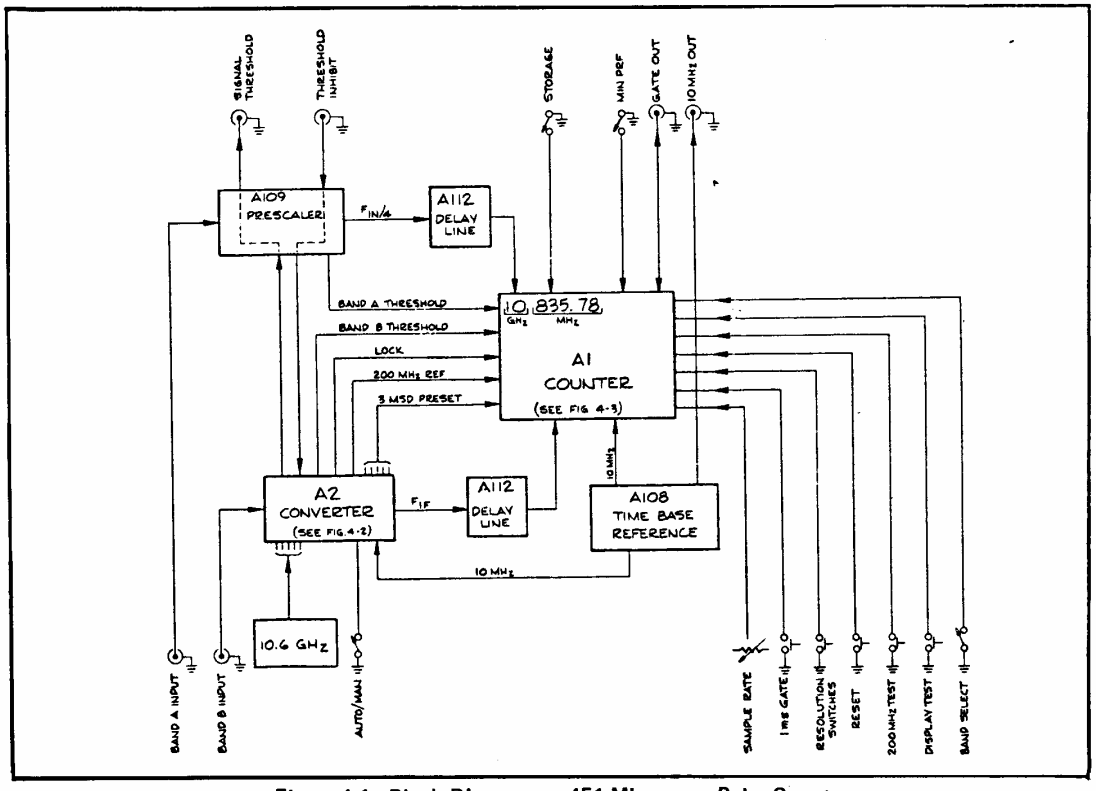


Figure 4-1. Block Diagram — 451 Microwave Pulse Counter

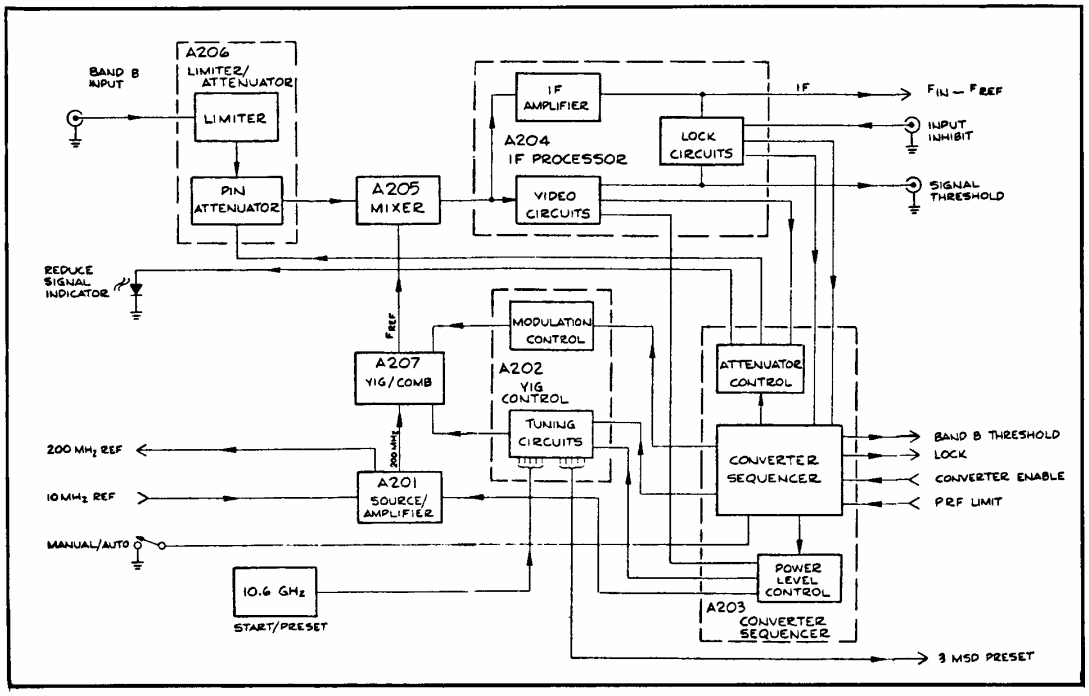


Figure 4-2. Block Diagram — 451 Pulse Counter - Converter (A2)

The 200 MHz reference is generated within Source/Amplifier (A201) by an LC oscillator which is phase-locked to the 10 MHz Time Base Oscillator (A108) within the 451. This reference is amplified to produce up to one watt of output power to drive the comb generator section of A207. A second output at 200 MHz is used to generate the gate and test functions within the Direct Counter.

The RF input signal to the Converter section first passes through a Limiter/Attenuator (A206). The limiter portion of this module is a passive diode whose main function is to protect the Mixer (A205) against excessive input power. Protection at levels up to one watt peak or average is provided. The attenuator section contains a multistage, matched PIN diode serving two functions: (1) To provide a means of controlling the RF signal level to the Mixer, and (2) to act as a switch which shuts off the input signal during certain portions of Converter operation.

The mixer (A205) is another integrated microwave circuit assembly, containing a hybrid coupler, termination, mixer diode, and a DC return. The Mixer produces two output signals on a common line: (1) An IF signal equal in frequency to the difference between the RF signal and the reference signal; (2) a Video signal resulting from rectification of either the RF or reference input.

The IF and Video signals are separated in the IF Processor (A204). This assembly contains an IF amplifier, video amplifiers, threshold circuits, and LOCK circuitry. The output of the IF amplifier is the signal actually measured by the Direct Counter. It is also used by the LOCK circuitry to determine the correct reference frequency (comb line). The Converter is considered to be locked when a particular comb line mixes with the applied RF signal to produce an IF signal of proper amplitude and frequency.

The amplified Video output is used to generate three separate signals: two threshold, and one analog output. One signal, SIGNAL THRESHOLD, is used to detect the presence of sufficient RF signal to initiate operation of the Converter and enable the gate of the Direct Counter. The second threshold, ATTENUATOR CONTROL, is activated at a level approximately 7 dB above SIGNAL THRESHOLD, and causes the attenuator to reduce the input signal level. The third signal is an analog output corresponding to the amplitude of the reference signal, and is used in the process of stepping from one comb line to another.

YIG control board (A202) contains all the functions necessary to step the YIG filter to the proper comb line. The primary circuits are a YIG Driver to supply the required current, a digital-to-analog converter (DAC) to set the approximate center frequency, and a centering circuit to precisely center the YIG filter passband on a comb line. The centering process involves modulating the YIG center frequency via an auxiliary modulation coil in the YIG structure. The modulation circuitry is also located on the YIG Control PC board.

The remaining major assembly in the Converter is the Converter Sequencer (A203). This assembly contains the power level control function to set comb line amplitude, the attenuator control function, and the Converter Sequencer which acts as the major control unit for the entire Converter (A detailed operational sequence is given in Section 8).

350 MHz DIRECT COUNTER

After an RF signal is translated into the range below 325 MHz, the frequency is determined by the 325 MHz Direct Counter. This is accomplished by accumulating the number of cycles of the signal which occur within a precisely determined time interval. This interval is based on the frequency of the Time Base Oscillator. In the 451, the total time intervals used are 100 microseconds and 1 millisecond. In order to measure narrow pulses to a resolution of 10 kHz, it is necessary to add together the number of cycles counted in each of a large number of pulses, until the required total time interval is obtained.

The Direct Counter consists of several major functional blocks as shown in Figure 4-3. Input signals are applied to High Frequency board (A106), where they are processed into a standardized signal suitable for counting. This signal then passes through the counter gate to the first decade of the counting chain, which accumulates the input count. The output of this decade goes to the Count Chain (A103) which contains the remaining six decades. A103 also includes the storage unit which holds all the digital information of the previous reading.

Information display is controlled by Count Chain Control (A102), which contains all the required multiplexing circuitry to drive the Display (A110). The logic to suppress leading zeros on the display is also on A102.

Overall control of the 451 Counter is performed by the Control board (A104). This assembly generates the counter operating sequence, and interfaces with most of the operating controls as well as the Converter and Prescaler.

GATE GENERATOR

The remaining function of the counter, that of generating a precision gate, is accomplished by the Gate Generator (A105). This function is considerably more difficult for pulsed signals than it is for CW signals, and it is on this function that the overall accuracy of the 451 depends. Two separate operations are performed. The first is to supply a GATE to the High Frequency board which is present only when an input signal is also present. The second is to accumulate the total time during which the GATE is applied, until 100 microseconds (or 1 millisecond) is reached.

The first operation requires that the GATE begin after the signal is present at A106, and end prior to the end of the signal. This is accomplished by generating a GATE approximately 30 nanoseconds shorter than the RF signal (as determined by the SIGNAL THRESHOLD level). The arrival time at A106 of the IF from the Converter (or Prescaler), is then controlled by a delay line so the GATE will fall entirely within the IF pulse.

The second operation is accomplished by counting clock pulses whenever the GATE is open, until a total time of 100 μs (or 1 ms) is obtained. This requires that each GATE opening is for an exact integral number of clock pulses. A 200 MHz clock is used for this, causing the GATE width to be increased in 5 ns steps until a total of 20,000 (or 200,000) clock pulses is accumulated.

ACCURACY

In the case of a CW measurement, absolute accuracy is determined almost entirely by the Time Base Reference frequency accuracy. In turn, this accuracy is a function of initial calibration and reference stability with time and temperature.

The remaining inaccuracy is the digital counting error, specified as ± 1 count, and is normally insignificant in CW measurements. It results from the fact that the number of periodic events that occur in a fixed time interval can vary by one, depending upon the phase of the signal.

When considering pulse measurement accuracy the digital counting error can become highly significant, especially for narrow pulses. This results from the fact that the error is a random error, which occurs every time the GATE is opened. Since the error is random, it is subject to statistical fluctuations. This averaging

error is proportional to $\sqrt{N}$, where N is the number of times the GATE is opened during a measurement. This, in turn, can be related directly to pulse width:

$$\text{Averaging Error (RMS) for 100 } \mu\text{sec gate} = \frac{100 \text{ (or 30) kHz}^{*}}{\sqrt{PW \cdot .03}}$$

PW = Pulse width in microseconds.

* 30 kHz with 1 ms gate, 200 (or 60) kHz in Band A.

Since the averaging error is random, its contribution to overall measurement error can be made arbitrarily small by mathematically averaging multiple readings.

The second source of error in pulse measurement is GATE error. This error results from a GATE which is not an exact integral multiple of the clock period. In the measurement of narrow pulses, GATE errors of small fractions of a nanosecond can be significant. Each time the GATE is opened, a fixed error is introduced. As a result, the error is proportional to the number of times the GATE is opened. This is a systematic error and will not average out as will the averaging error. The worst case GATE error, including all effects of frequency and temperature, is given by:

	Band B	**Band A**
Gate Error (max) =	$\frac{\pm 40 \text{ kHz}}{PW \cdot .03}$	$\frac{\pm 100 \text{ kHz}}{PW \cdot .03}$

PW = Pulse width in microseconds.

If necessary, GATE error at any particular frequency and pulse width, can be calibrated out of the counter.

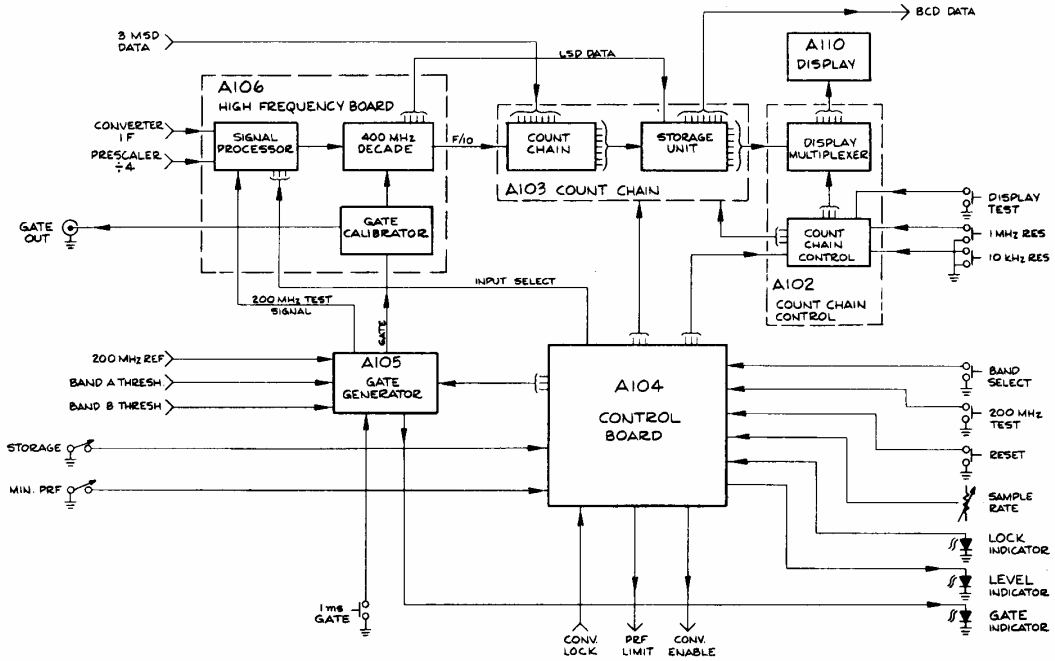


Figure 4-3. 451 Direct Counter (A1)

AN INTRODUCTION TO YIG FILTERS

Highly polished spheres of single crystal YIG (yttrium-iron-garnet), have a property called ferrimagnetic resonance. Basically, the ferrimagnetic resonance phenomenon can be explained in terms of spinning electrons creating a net magnetic moment in each molecule of a YIG crystal (see Figure A). Viewing the material microscopically, there is no net effect because the magnetic dipoles associated with each molecule are randomly oriented (see Figure B). The application of an external magnetic biasing field, H_{DC}, causes the magnetic dipoles to be aligned in the direction of the biasing field (see Figure C).

An RF field can be used to create an orthogonal magnetic force. If the frequency of the RF field coincides with the natural precession frequency, there is a strong interaction called ferrimagnetic resonance (Fig. D).

Figure E shows the basic elements of a YIG bandpass filter. The filter consists of a YIG sphere at the center of two loops. The two loops are perpendicular to each other and the DC biasing field, H_{DC}. One loop carries the RF input and the other the RF output. When the RF signal frequency is the same as the natural precession frequency of the YIG, there is strong coupling between the input and output loops. Thus RF can only pass through the YIG filter at resonance. The resonant frequency is a linear function of the magnetic biasing field, H_{DC}. Generally, H_{DC} is provided by locating the YIG spheres between the poles of an electromagnet, and tuned by varying the current to the magnetic coils.

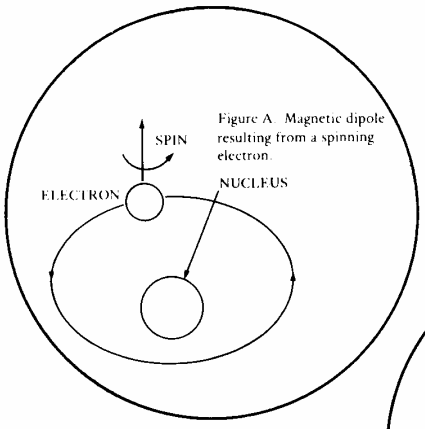


Figure A. Magnetic dipole resulting from a spinning electron.

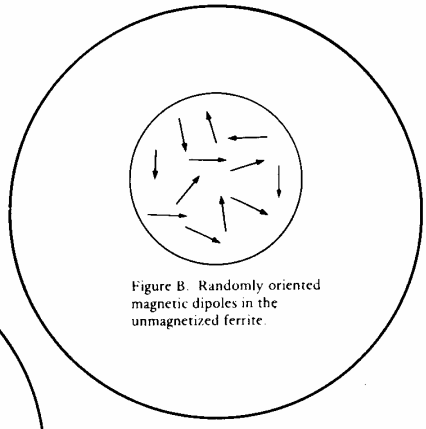


Figure B. Randomly oriented magnetic dipoles in the unmagnetized ferrite.

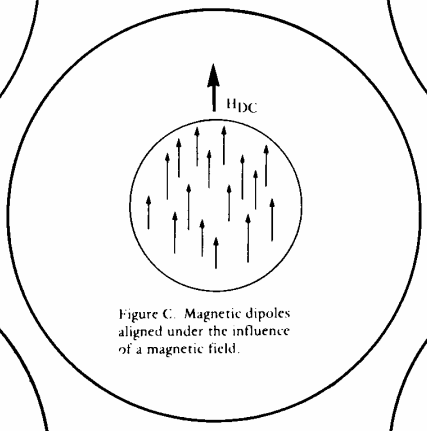


Figure C. Magnetic dipoles aligned under the influence of a magnetic field.

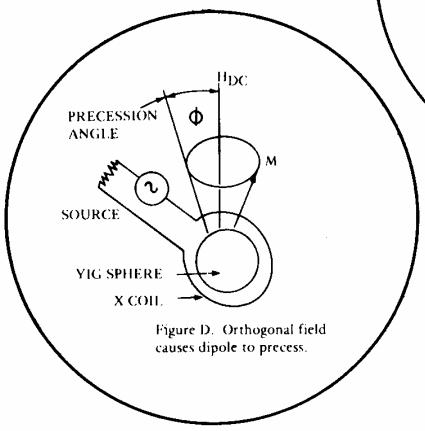


Figure D. Orthogonal field causes dipole to precess.

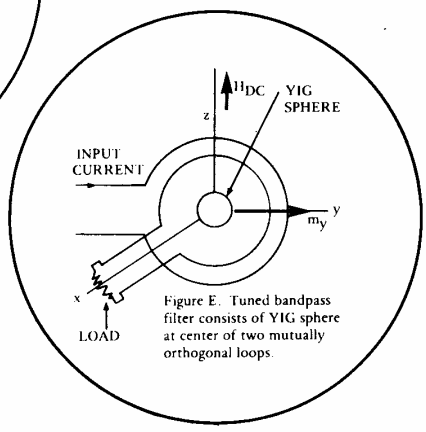


Figure E. Tuned bandpass filter consists of YIG sphere at center of two mutually orthogonal loops.

Section 5
Maintenance and Service

GENERAL

This section provides instructions, procedures, and information necessary to maintain, troubleshoot, and repair the 451.

FUSE REPLACEMENT

The counter uses one fuse, located in the POWER INPUT module on the rear panel. For proper operation, use only the fuse specified. Do not increase fuse rating or change fuse type. Power module PC board should display the correct nominal line voltage when installed in the module. TO CHANGE TO ANOTHER LINE VOLTAGE:

1. Slide open power module cover and rotate FUSE PULL to the left.

2. Select operating voltage by orienting PC board so nominal supply line voltage appears on the top left side of the PC board. Push board firmly into module slot. (NOTE: When board is completely inserted, only the selected operating voltage will be visible).

3. Rotate FUSE PULL back into normal position and insert fuse in holder, taking care to select correct fuse value. Close module cover.

4. For 100/120 VAC operation, use a 1.5 A, Slow-Blow, 3AB/MDX type fuse. For 220/240 VAC operation, use a 0.75 A, Slow-Blow, 3AB/MDL type fuse.

AIR CIRCULATION

During operation of the counter, the internal fan draws in cooling air through the vents in the rear panel. If these vents are blocked, the temperature inside the enclosure may rise to the point where counter stability is reduced, and component life shortened.

COUNTER SERVICING

Recommended Service Procedures:

1. To remove plug-in PC boards: Turn off power to counter. Ease PC board out of its socket by lifting up on board handles. Remove carefully to avoid placing strain on any connecting cables.

2. To unplug flat ribbon cables: Turn off power to counter. Remove PC board as necessary. Use an IC Extractor Tool (EIP P/N 5000094 or equivalent) to unplug flat ribbon connector.

3. To remove PCB socket locating key: Key must be turned 90° before removal from or re-insertion into socket to avoid contact damage. Use long-nose pliers for removal or insertion.

4. Internal cable and harness routing is shown both in Figure 8-1 and inside the top cover of the counter.

5. Circuit descriptions of PC board and modular assemblies are shown on the same pages (in Section 8) as the related schematic diagram and component layout.

6. Troubleshooting Trees shown later in this section are intended only as a guide, and do not describe every possible failure situation. To speed troubleshooting of a board, replace the board with a known good one.

7. A listing of recommended test equipment for servicing, calibration, and performance testing, is given in Table 5-1. Other equipment may be used provided performance equals or exceeds that listed.

SERVICING PRECAUTIONS

1. The following assemblies should be replaced instead of being serviced in the field due to the specialized test equipment and procedures required for recalibration: Source/Amplifier (A201), IF Processor (A204), Mixer (A205), Pin Limiter Attenuator (A206), Yig Comb Generator (A207).

2. If the following assemblies are repaired or replaced either at EIP or in the field, recalibration in the associated counter will be required for proper operation: Gate Generator (A105), High Frequency (A106), YIG Control (A202), Converter Sequencer (A203), Mixer (A205), Pin Limiter Attenuator (A206), Yig Comb Generator (A207).

CAUTION

DO NOT ATTEMPT REPAIR OR DISASSEMBLY OF THE FOLLOWING COMPONENTS: MIXER (A205), PIN LIMITER/ ATTENUATOR (A206), YIG COMB GENERATOR (A207), OR TCXO TIME BASE OSCILLATOR (ON A108).

FACTORY SERVICE

If the counter is to be returned to EIP for service or repair, be sure to include the following information with the shipment:

1. Name and address of owner.

2. Model, CCN and complete serial number of counter.

3. A complete description of trouble (e.g. Under what conditions did trouble occur? What was the signal level? What associated equipment was attached or connected to the counter? Did that equipment fail too?).

4. Name and telephone number of someone familiar with the problem who may be contacted by EIP for any further information if necessary.

5. Shipping address to which counter is to be returned. Include any special shipping instructions.

6. Pack the counter for shipment as follows:

   A. Wrap the counter in plastic or heavy kraft paper, and repack in the original shipping container (if still available) using the original packing material.

B. If the original container and packing material are no longer available, use a heavy (275 lb. test) double-walled carton, with approximately 4" of suitable packing material between the inner and outer walls, with additional packing material as required between the counter and the inner carton. Seal with strong filamentary tape or strapping.

C. Mark shipping container to indicate that it contains fragile electronic instruments. Ship to EIP at address shown on title page of this manual.

TROUBLESHOOTING

MALFUNCTION AT TURN ON

If the counter fails to turn on (no display, no fan, etc.), make the following checks:

1. Power module PC board correctly inserted and fused.
2. Power cord plugged into counter and into active AC power source.
3. POWER switch at "ON" position(button depressed and green indicator showing).
4. PC boards and connectors are properly engaged.
5. Power supply voltages correct (measure at A100J3); refer to Section 6 for acceptable tolerances.

FAILURE TO INDICATE ALL ZEROS

If counter turns on, but fails to indicate all zeros with no applied signal, check that:

1. No RESOLUTION switches are depressed.
2. Rear panel MIN PRF switch is in 50 Hz position.
3. PC boards and connectors are properly engaged.
4. Power supply voltages correct.
5. Perform Visual Display Test by pressing DISPLAY TEST switch on front panel. Display should show the numeral "8" in all decade positions.
6. If counter fails the Visual Display Test refer to Troubleshooting Tree Figure 5-4. If counter displays all eights but a digit is missing, refer to Figure 5-5. If the display does not show all zeros when it should, refer to Figure 5-6.

MALFUNCTION IN SELF TEST

If counter turns on, but fails to indicate a reading of 200.00 (200 MHz) in the TEST mode, check that:

1. Counter indicates all zeros with no applied signal.
2. PC boards and connectors are properly engaged.

3. Power supply voltages correct.

4. Counter passed Visual Display Test (paragraph 5-16).

5. Refer to Figure 5-7.

MALFUNCTION IN BAND A (OPTION P2)
(300 MHz to 950 MHz)

If counter fails to read frequency correctly, check that:

1. BAND SELECT switch is in the Band A position.

2. A signal of the proper level and frequency range is applied to the Band A input connector.

3. If signal input is correct, counter should indicate all zeros when signal is removed.

4. Counter passes Visual Display Test.

5. Counter operates correctly in TEST mode.

6. Refer to Figure 5-8.

MALFUNCTION IN BAND B
(925 MHz to 18 GHz)

If the counter fails to read frequency correctly check that:

1. BAND SELECT switch is in the Band B position.

2. A signal of the proper level and frequency range is applied to the Band B input connector.

3. If signal input is correct, counter should indicate all zeros when signal is removed.

4. Counter passes Visual Display Test.

5. Counter operates correctly in TEST mode.

6. YIG Control (A202) and Converter Sequencer (A203) PC board and co-ax connectors are properly engaged.

7. Refer to Figure 5-9.

MODULE FAILURE VERIFICATION

SOURCE AMPLIFIER POWER CHECK

1. Turn off counter power. Remove cable from A201J2.

2. Connect a co-ax cable to A201J2 which is connected to a 30 dB, 1 watt attenuator. Output of the attenuator should be fed to a broadband calibrated detector.

CAUTION: 1 watt at 200 MHz can appear at A201J2.

3. Turn on counter. Set counter to Band B.

4. Apply a +5 dBm, 1-18 GHz signal to the Band B input connector.

5. Check that Source/Amplifier (A201) has correct power supply voltages, 10 MHz Reference, and Power Reference inputs.

6. Connect dual-trace scope Channel A to A201FL1 (2 V/div), and Channel B to detector output.

7. Set Channel B sensitivity for full scale deflection at 0 dBm into detector (1 W at A201J2).

8. Channels A and B should have similar waveforms, with maximum detector output approximating 1 watt at A201J2 (see Figure 5-1).

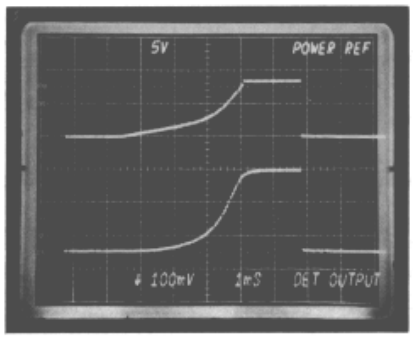


Figure 5-1. Source/Amplifier Power Ref/Detected Output

SOURCE AMPLIFIER SPURIOUS SIGNAL CHECK

1. Connect A201J2 through a 30 dB, 1 watt attenuator to a spectrum analyzer.

2. Remove wire connected to A201FL1. Connect FL1 to a variable 0 to +8 VDC source. Vary the DC level to FL1 and observe the spectrum from 100 MHz to 400 MHz for spurious signals.

FRONT END CHECK

1. Turn off counter power. Remove Converter tray (A2), and cover from IF Processor module (A204).

2. With Converter tray out of counter, reconnect tray to counter power at A200P1. Turn on power to counter.

3. Apply a signal in the 1-18 GHz range at +5 dBm to the Band B input connector.

4. Remove cable at A204J4 (Attenuator Control), then depress RESET button.

5. Monitor IF input at A204J8; a DC voltage between 50 to 250 mV should be indicated. If output is

not in this range, either the Mixer (A205) or the Limiter/Attenuator (A206) is faulty.

CAUTION

Static discharge and/or voltage present at the input of some DVM's can damage the mixer diode. Connect cables to test equipment, and discharge the center conductor before measuring the output at J8.

6. Re-install and reconnect above assemblies if OK.

MIXER CHECK

1. Turn off counter power. Remove screws holding IF Processor (A204) to Converter tray (A2).

2. Remove co-ax inputs to Mixer (A205).

3. Unplug and remove IF Processor (A204).

4. Remove the two screws holding Mixer to IF Processor, and remove the Mixer.

5. Apply a 0 dBm signal in the 1-18 GHz range to the Mixer RF input port (see Figure 5-3). Monitor DC output with oscilloscope at IF converter port (connector that plugs into IF Processor). A DC voltage between 50 and 250 mV should be indicated.

6. Re-install and reconnect above assemblies if OK.

PIN LIMITER/ATTENUATOR CHECK

1. Turn off counter power. Remove Converter tray (A2).

2. Remove PIN Limiter/Attenuator (A206) from tray.

3. Disconnect PIN Limiter/Attenuator from Converter Sequencer (A203). Unplug co-ax input to Mixer (A205).

4. Apply a +7 VDC to A206P1 pin 4, and -8 VDC to A206P1 pin 1, with common to ground lug on module.

5. Apply a 0 dBm signal in the 1-18 GHz range to the type N connector. Output should be between -7 dBm and -8 dBm.

6. Re-install and reconnect above assemblies if they have checked out properly.

YIG COMB GENERATOR CHECK

1. Select Band B, Auto Sweep, and 0 GHz start frequency.

2. Apply 0 dbm 1 to 18 GHz CW signal to Band B.

3. Carefully remove co-ax cable connecting YIG Comb Generator output (A207J1) and Mixer

4. Connect a 1-18 GHz broadband calibrated detector to A207J1. The detector output should match Figure 5-2.

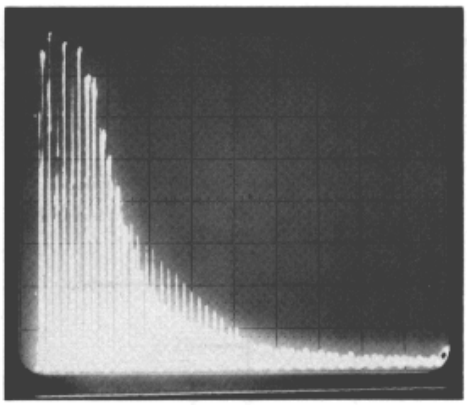
5. Check that the YIG Comb Generator (A207) has the proper inputs:

   A. 0 to 2 volt positive-going ramp at YIG Control A202J3 pin 5.

   B. RF power at A207J2 (from Source/Amplifier).

   C. The level indicator light is lit.

NOTE: Due to the special test equipment required to thoroughly test the performance of the YIG Comb Generator, the above check is adequate only as an indication of a complete failure.



20m Volts/Div 100 msec

Figure 5-2. YIG Comb Generator Detected Output

IF PROCESSOR CHECK

1. Turn off counter power. Disconnect both co-ax inputs to Mixer (A205).

2. Remove IF Processor (A204) from Converter tray. Keep A204P1 (power plug) connected to A200J1.

3. Connect IF Processor to two signal generators as shown in Figure 5-3. Terminate A204J3 in 50 ohms.

4. Turn on counter.

(Signal Threshold Detector Check)

5. Connect oscilloscope 10X probe to A204J6 ($\overline{\text{Band B Threshold}}$).

6. Set LO signal source for 1 GHz ± 1 MHz at -16 dBm, and apply to LO Mixer port (see Figure 5-3).

7. Set RF signal source to 1.2 GHz. Vary RF level from -30 to -20 dBm. A204J6 should go low before RF level reaches -21 dBm.

(Converter Inhibit Check)

8. Set RF source to - 20 dBm. Terminate A204J5 in 50 ohms.

9. Verify that A205J6 is at an ECL high (-0.8 VDC). Remove 50 ohm termination.

(Attenuator Check Control)

10. Connect oscilloscope Chan. A 10X probe to A204J4 (Attenuator Control), and Chan. B 10X probe to A204J1 (Converter Threshold).

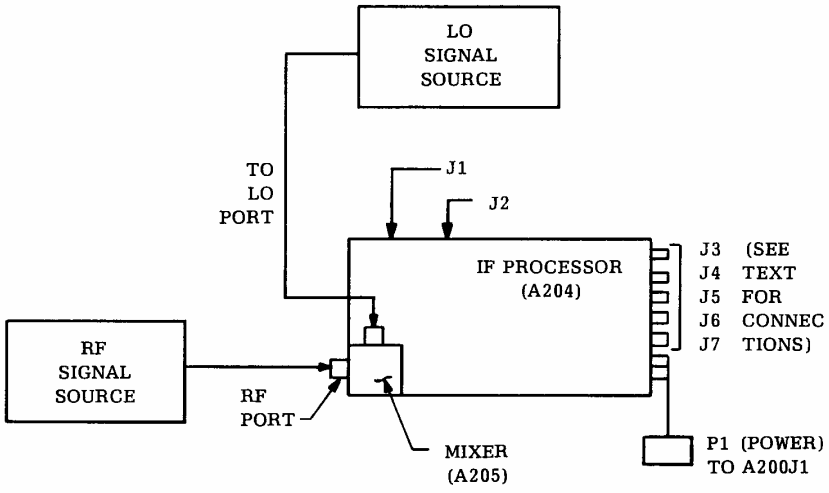


Figure 5-3. Test Set-Up IF Processor (A204)

11. Vary RF source level from below -20 dBm to above -10 dBm. Observe the following:

    A. When RF level is below -20 dBm, A204J1 (ECL level) and A204J4 (TTL level) are both high.

    B. As the level of the RF source is increased, A204J1 goes low. Note this level.

    C. A204J4 goes low 6 to 8 dB higher than A204J1 went low.

(In-Band Detector/Lock Logic Check)

12. Connect Channel A 10X probe to A204J7 (Lock).

13. Set RF source to -20 dBm with 1 kHz square wave modulation. Tune RF source from 1.4 GHz down to 1.0 GHz. Check that the Lock signal goes high (ECL level) at 1.327 GHz ± 3 MHz. Note this frequency.

14. Tune RF source from 1.0 GHz to 1.4 GHz. Check that the Lock signal goes high at 1.100 GHz ± 5 MHz, and then goes low at a frequency 25 to 35 MHz higher than that measured in step 13 above.

15. Set RF source to 1.2 GHz at -30 dBm. Modulate RF source with 1.5 microsecond pulses at a 20 kHz repetition rate.

16. Connect Channel A 10X probe to A204J2 (Detected Modulation). Output should be 1.5 microsecond positive pulses at 1.6 to 2.4 V amplitude (referenced to -6 volts).

RECOMMENDED TEST EQUIPMENT

EQUIPMENT DESCRIPTION	CRITICAL PARAMETERS	
SIGNAL SOURCE		
1. 300 MHz – 1.4 GHz	Frequency dial accuracy :	10 MHz from 1 to 500 MHz 2%*from 500 to 1400 MHz
	Spurious Signals :	26 dBc
	Residual FM :	<15 kHz
	RF output Amplitude :	+10 to -80 dBm
	Impedance :	50 ohms
2. 1 GHz – 18 GHz	RF power :	Variable over 0 to +10 dBm
	Wide Sweep Mode:	Linear sweep from F start to F stop over all or any part of range
	CW Mode :	Full range tuning
	Trigger Modes:	Internal recurring, line sync, manual or external
3. Pulse Modulation	Frequency range:	300 MHz to 18 GHz
	Rise time :	≤10 nsec
4. Pulse Generator	Polarity :	Two separate channels, one positive going, one negative going with seperately adjustable offset and amplitude
	Rep. rate :	1 Hz to 50 MHz, adjustable
	Width :	10 nsec to 1 sec
	Delay :	10 nsec to 1 sec
	Amplitude :	Separate 10, 5, and 1 volt ranges with continuous 10:1 adjustment
	Output Z :	50 ohms
	Rise/fall times :	<3.5 nsec
OSCILLOSCOPE, DUAL TIME	Bandwidth :	≥ 200 MHz
	Vert. Deflection Factor :	2 mV to 5 V per division
	Deflect. Factor Accuracy:	± 3%
	Sweep range :	0.5 sec/div. to .01 msec/div. in 24 steps, 1,2,5 sequence
DIGITAL VOLT METER	Number digits:	4½
	Basic accuracy:	.01%
	Range:	0 to 1000 volts
	Resolution:	AC– .01% of range 10 micro volts on 0.1 V range DC– 10 micro volts on 0.1 V range
POWER METER	Frequency range:	10 MHz to 18 MHz
	Power range:	10 microwatts to 10 milliwatts ranges in 1, 3, 10 sequence. Also calibrated in dBm from -20 to +10
	Accuracy :	+ 1% of full scale
THERMISTER MOUNT	See Power Meter	
CRYSTAL DETECTOR	Frequency range:	10 MHz to 18 GHz
20 dB DIRECTIONAL COUPLER	Frequency range:	At least 1.7 to 12.4 GHz
	Directivity:	≥ 25 dB
VARIABLE LINE VOLTAGE SOURCE	Output:	115 VAC at 100 Watts
EXTENDER CARD	EIP part number 2020041-01	
ADAPTER CABLE (SMC to BNC)	EIP part number 2040015-01	
MISC. ATTENUATORS, ADAPTERS, AND CABLES		

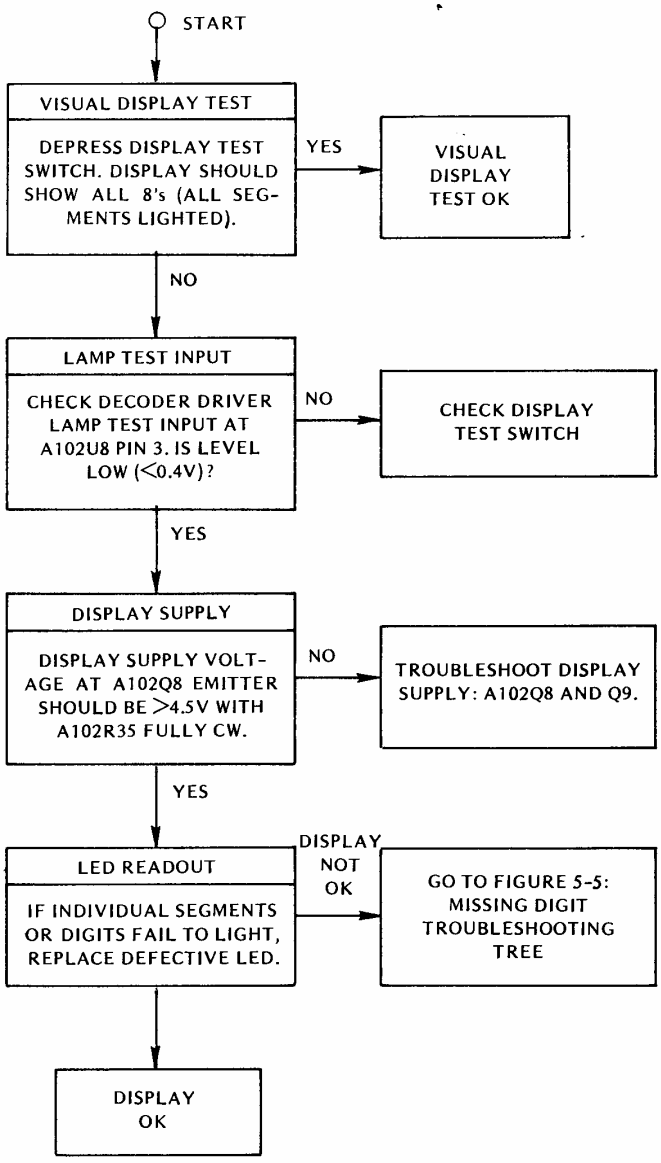


Figure 5-4. Visual Display Test

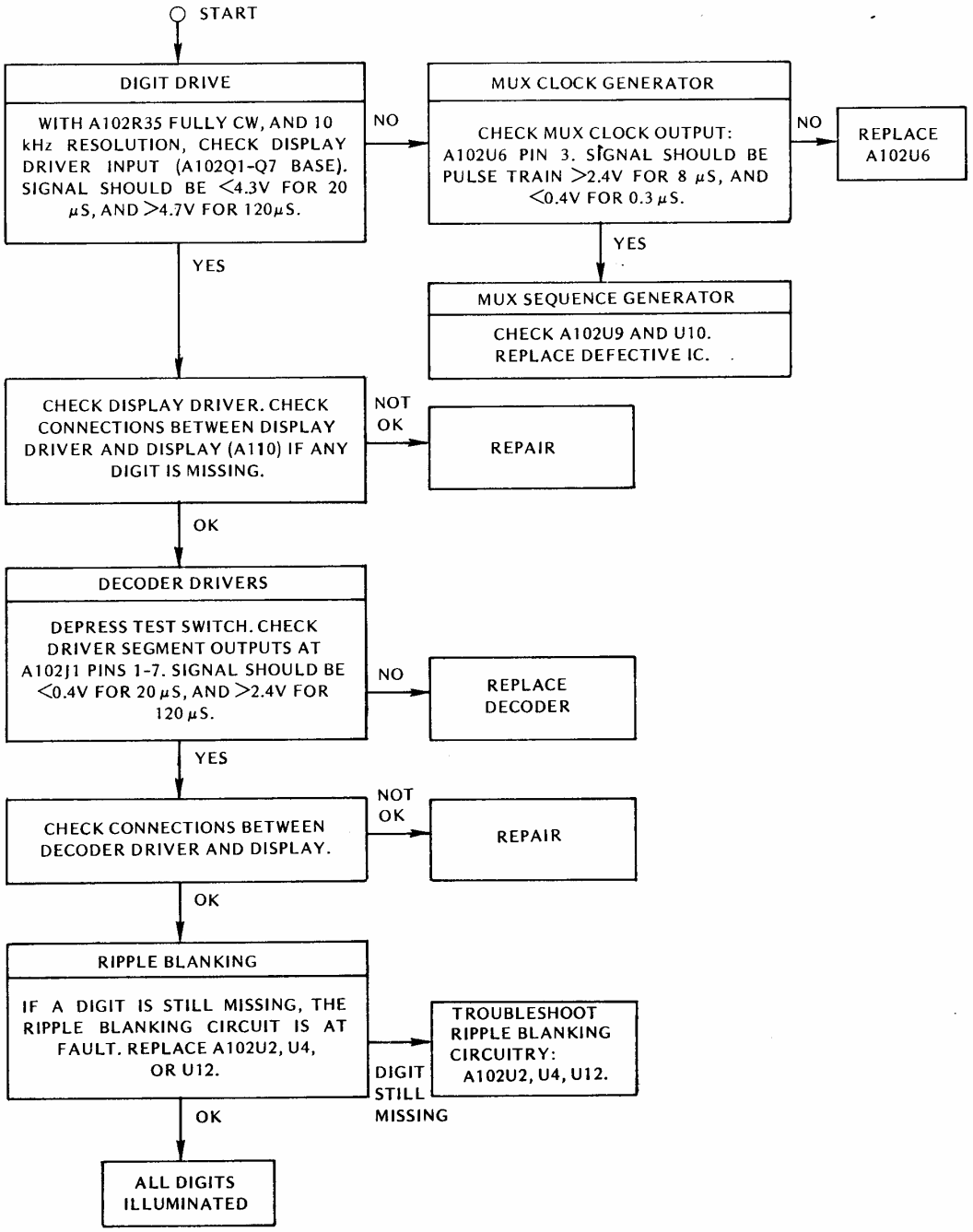


Figure 5-5. Missing Digit

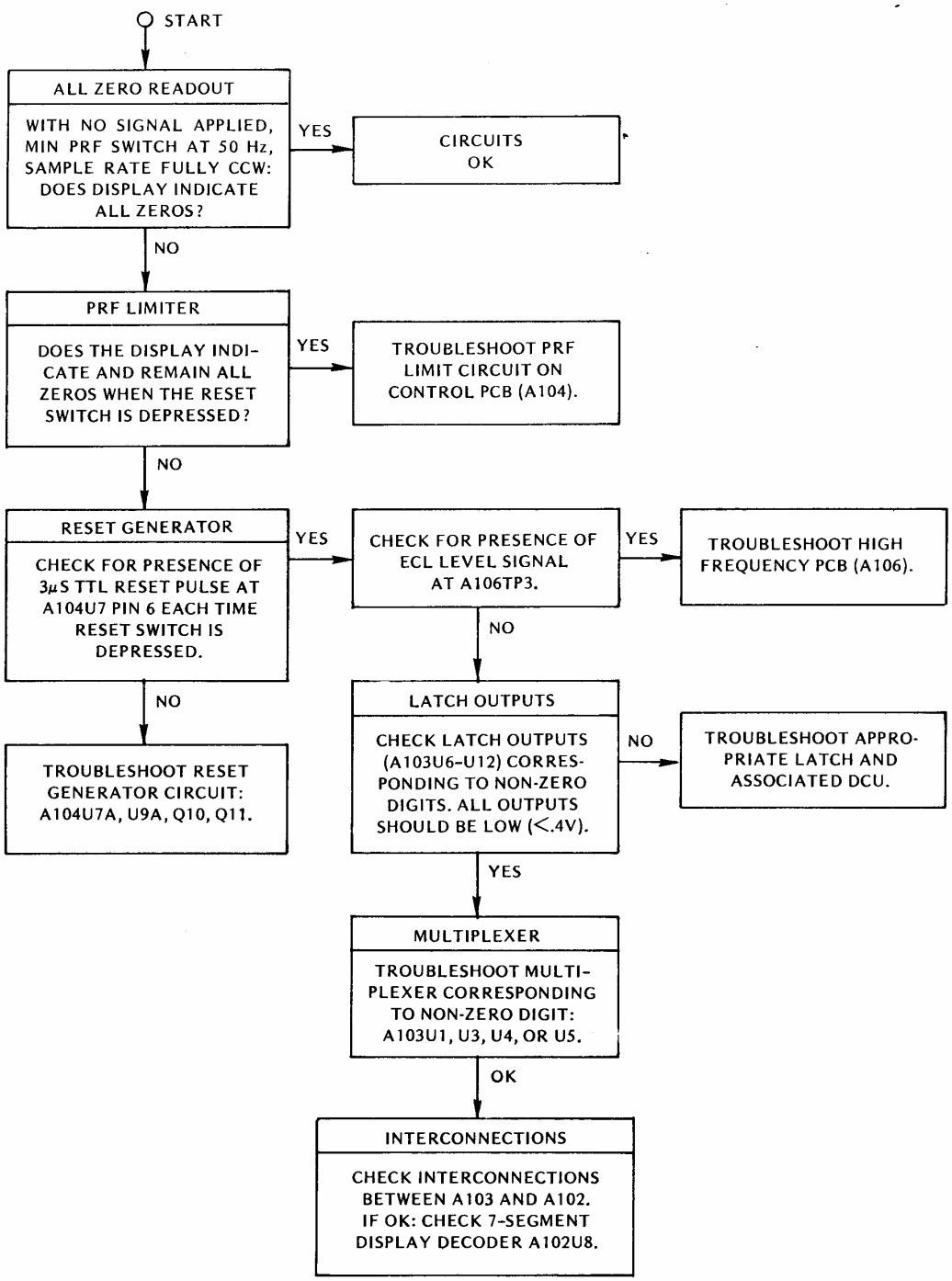


Figure 5-6. Non-Zero Display

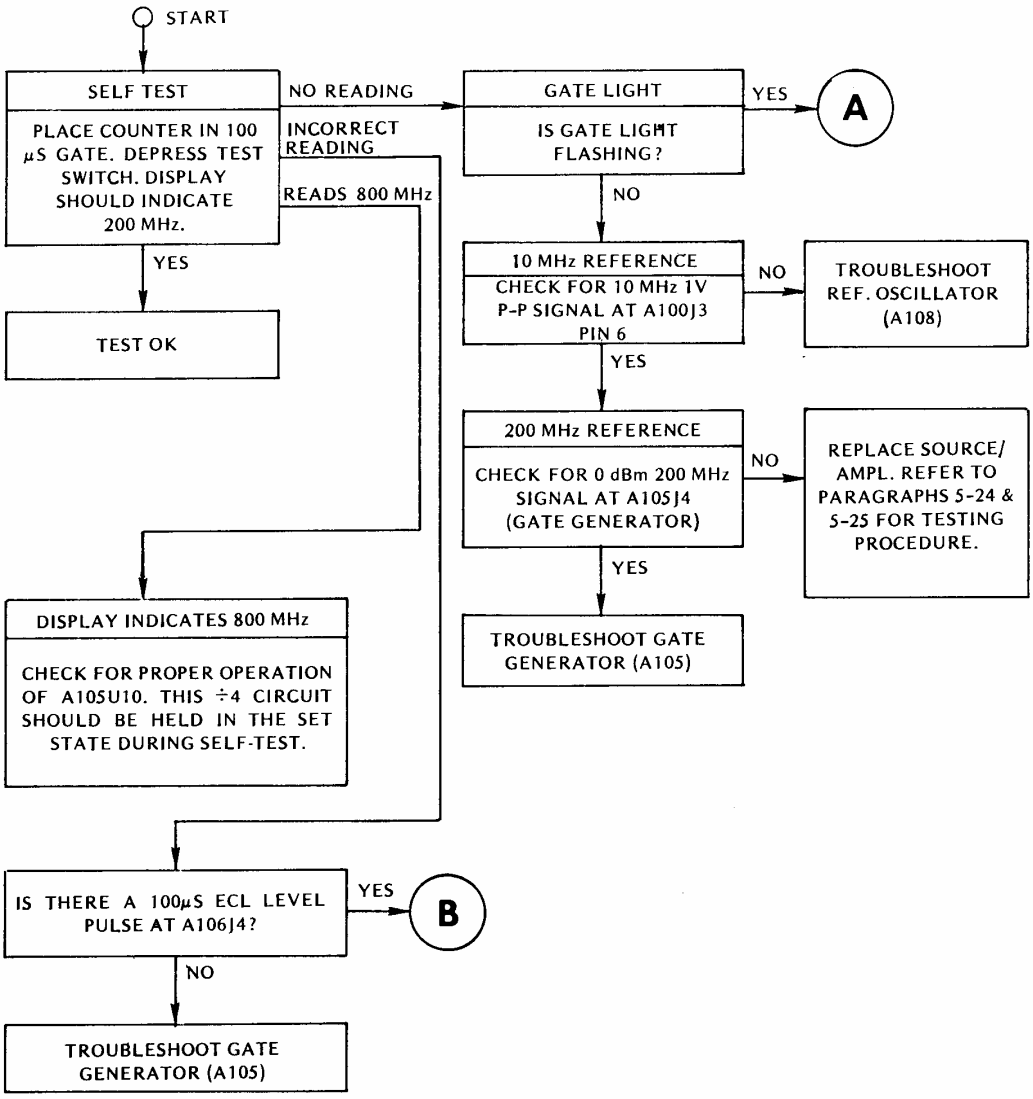


Figure 5-7. Self-Test

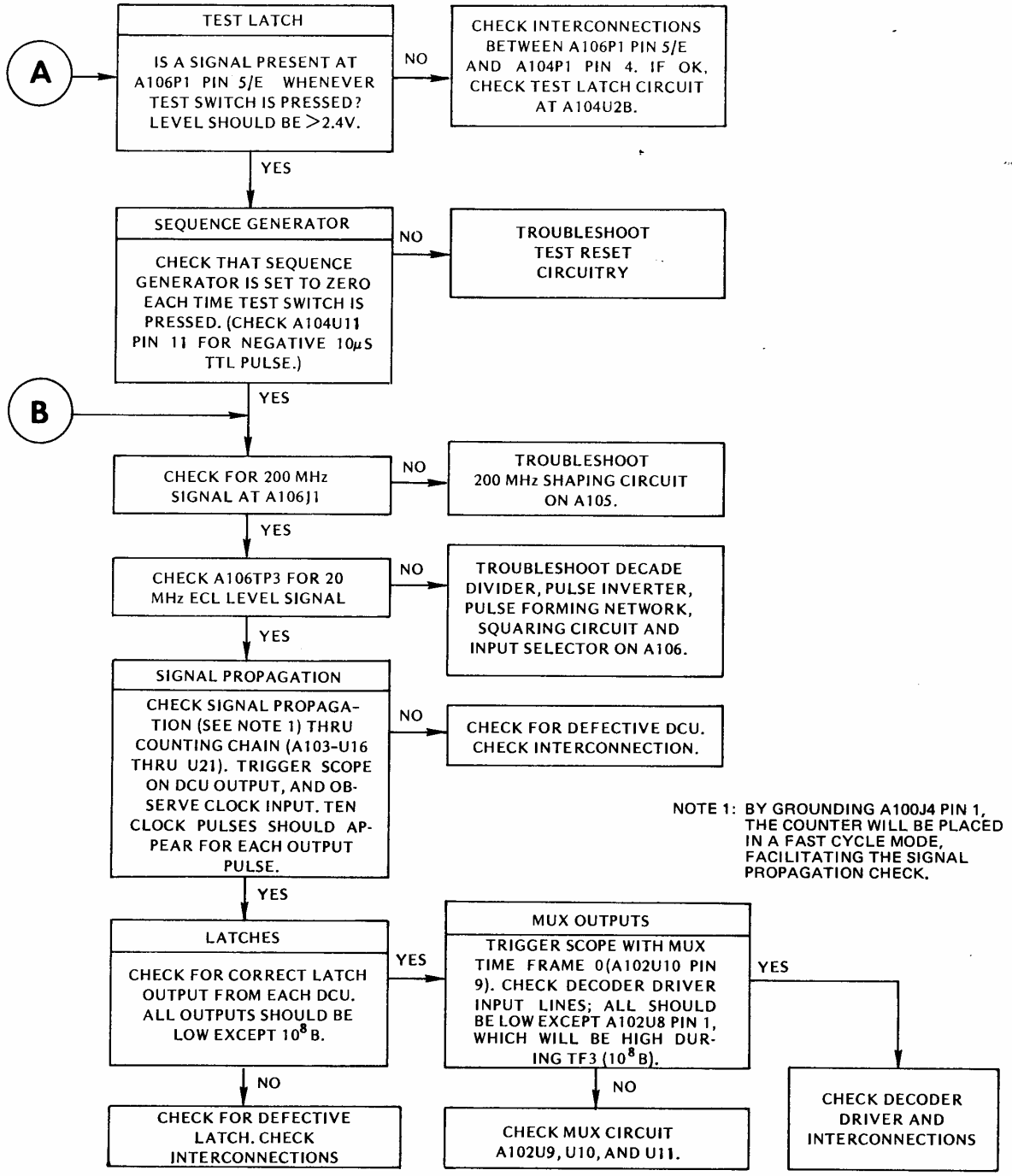


Figure 5-7. Self-Test
(Continued)

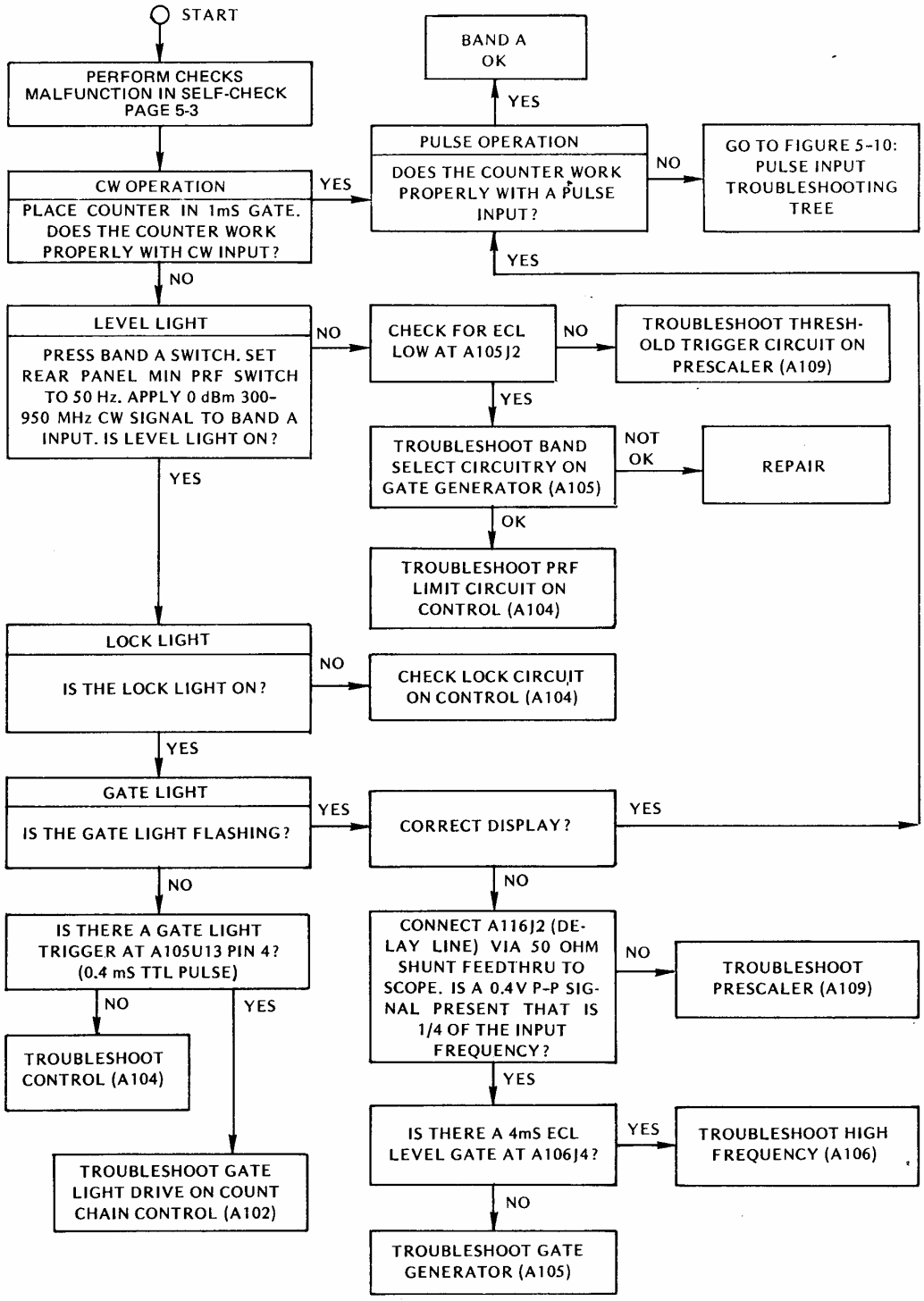


Figure 5-8. Band A (Opt P2)
300 MHz - 950 MHz

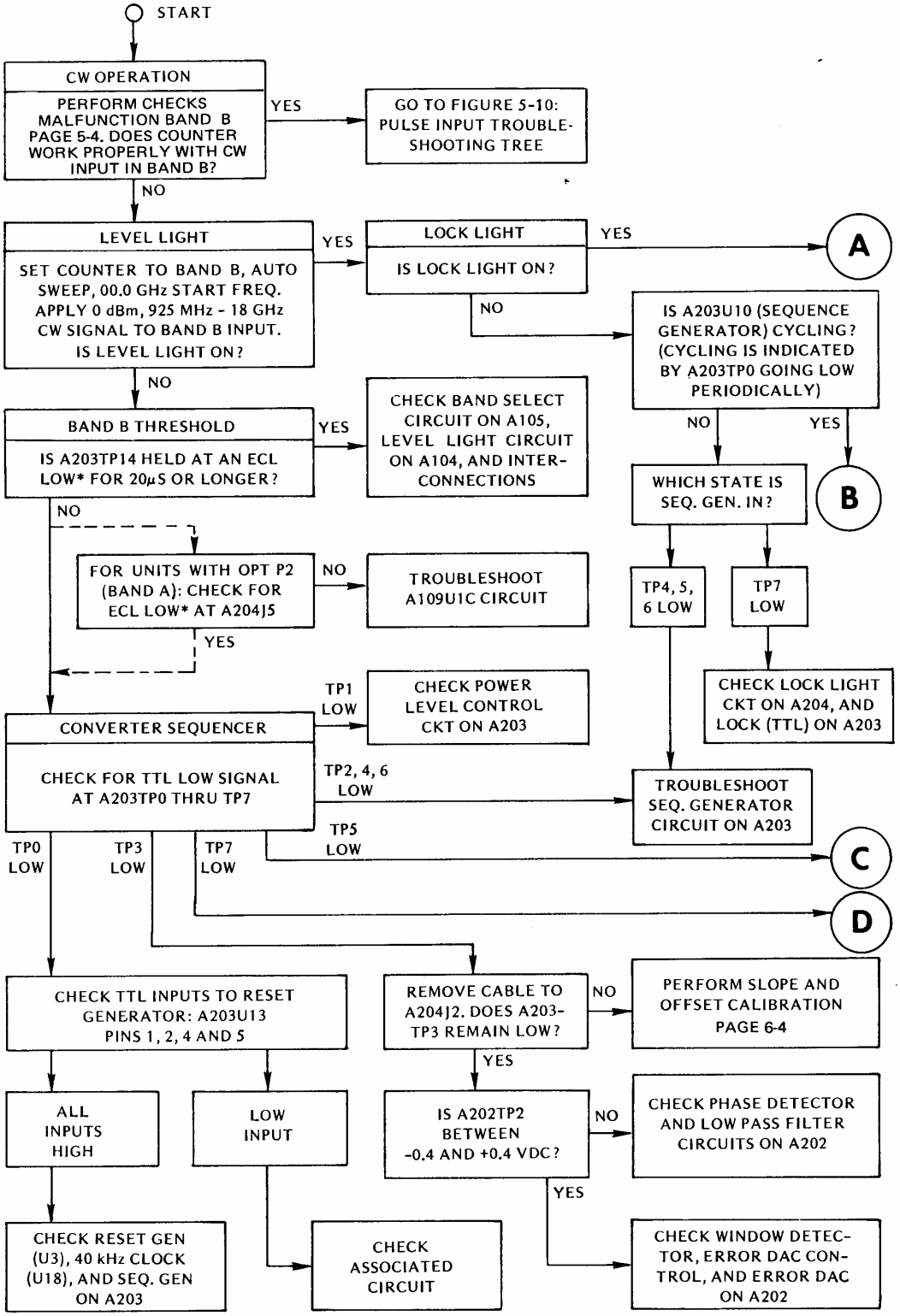


Figure 5-9. Band B (Converter)
925 MHz - 18 GHz

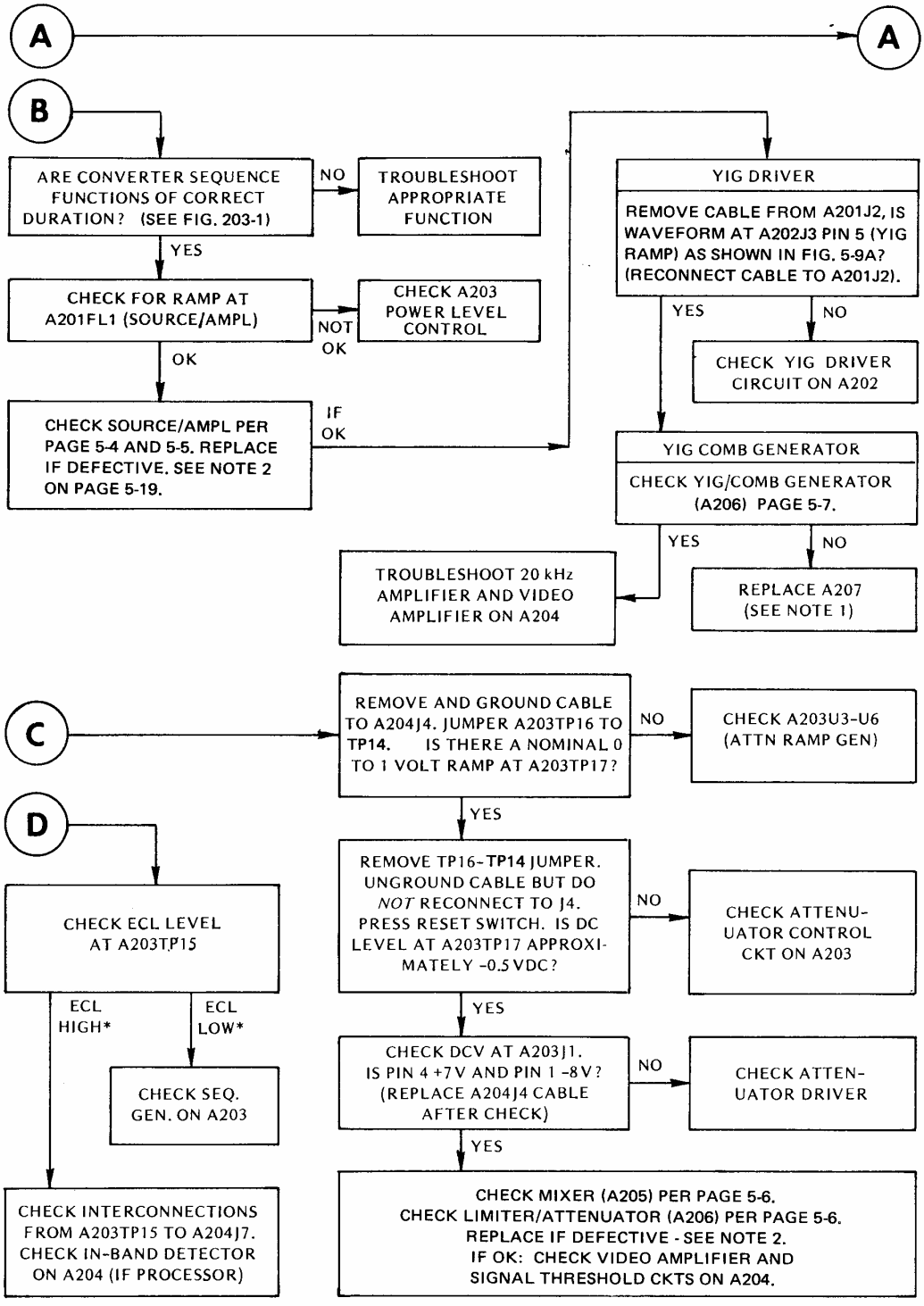
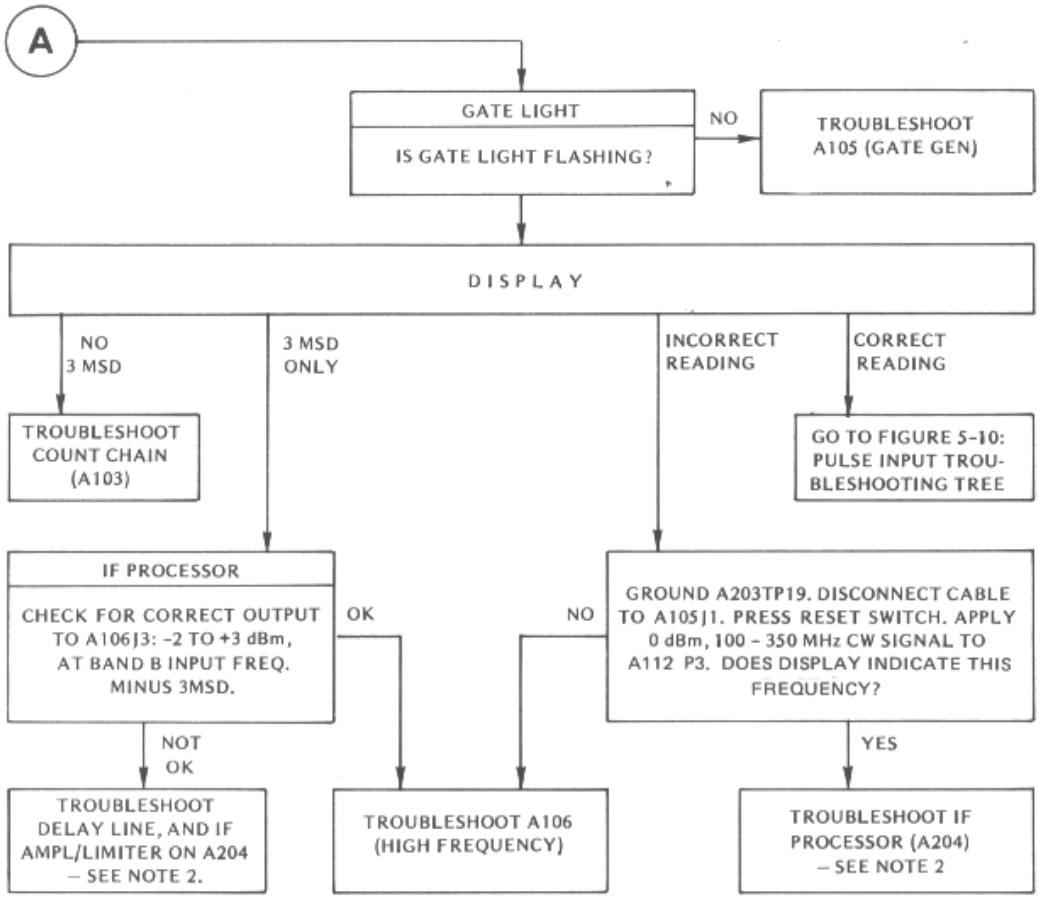


Figure 5-9. Band B (Converter)
925 MHz - 18 GHz
(Continued)



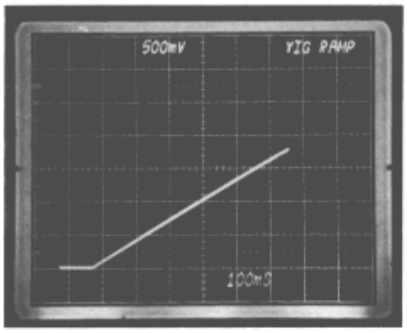


FIGURE 5-9A. YIG RAMP

* ECL HIGH = -0.8 VDC, ECL LOW = -1.7 VDC.

NOTE 1: THE FOLLOWING ASSEMBLIES SHOULD BE REPLACED IF DEFECTIVE, NOT REPAIRED. (SEE PAGE 5-1 FOR COUNTER SERVICING.) A205 MIXER, A206 LIMITER/ATTENUATOR, A207 COMB GENERATOR.

NOTE 2: THE FOLLOWING ASSEMBLIES REQUIRE SPECIAL CALIBRATION PROCEDURES AND SHOULD BE REPLACED IF DEFECTIVE, NOT REPAIRED. (SEE PAGE 5-1 FOR COUNTER SERVICING.) A201 SOURCE AMPLIFIER, AND A204 IF PROCESSOR.

Figure 5-9. Band B (Converter)
925 MHz - 18 GHz
(Continued)

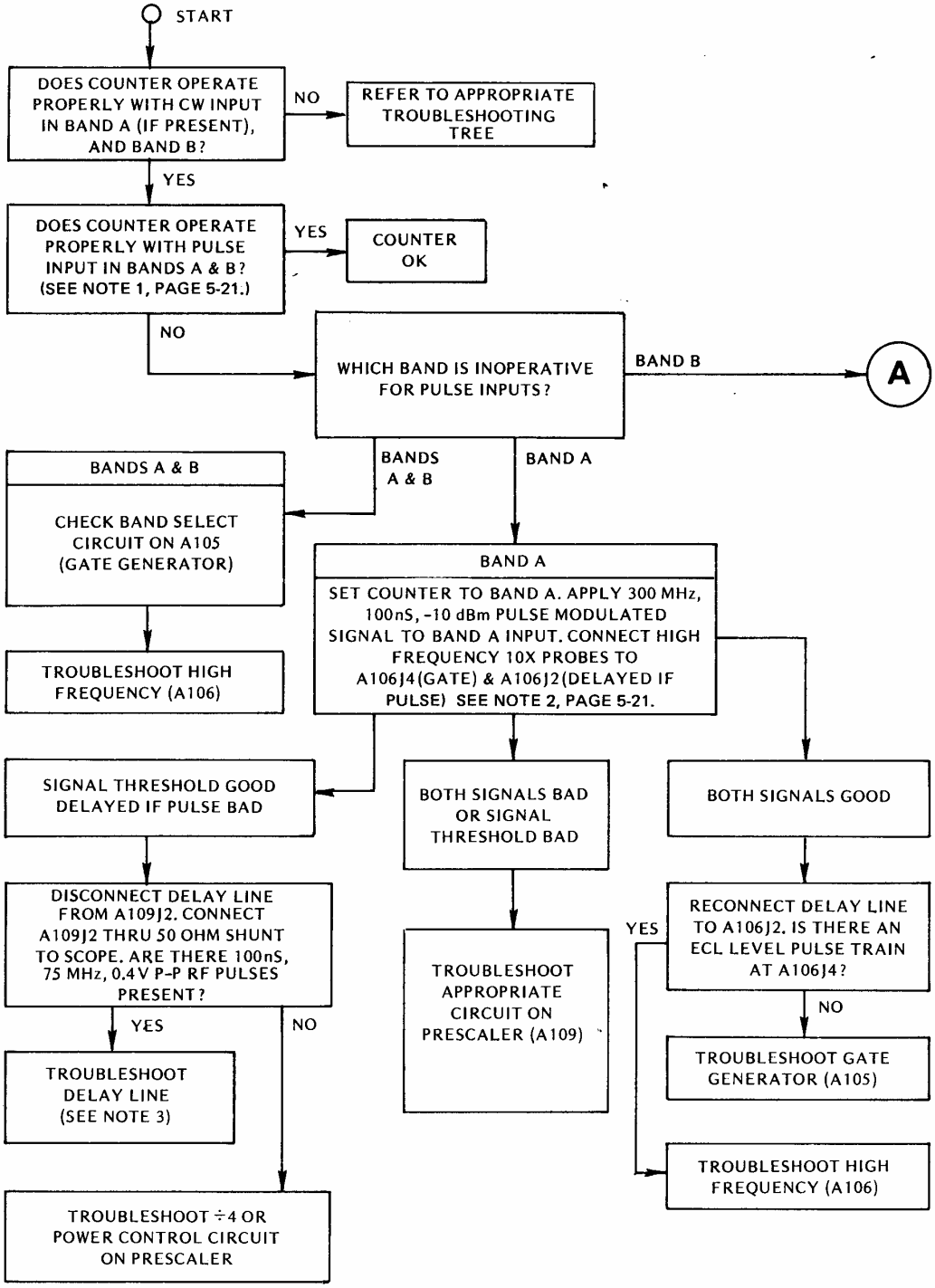
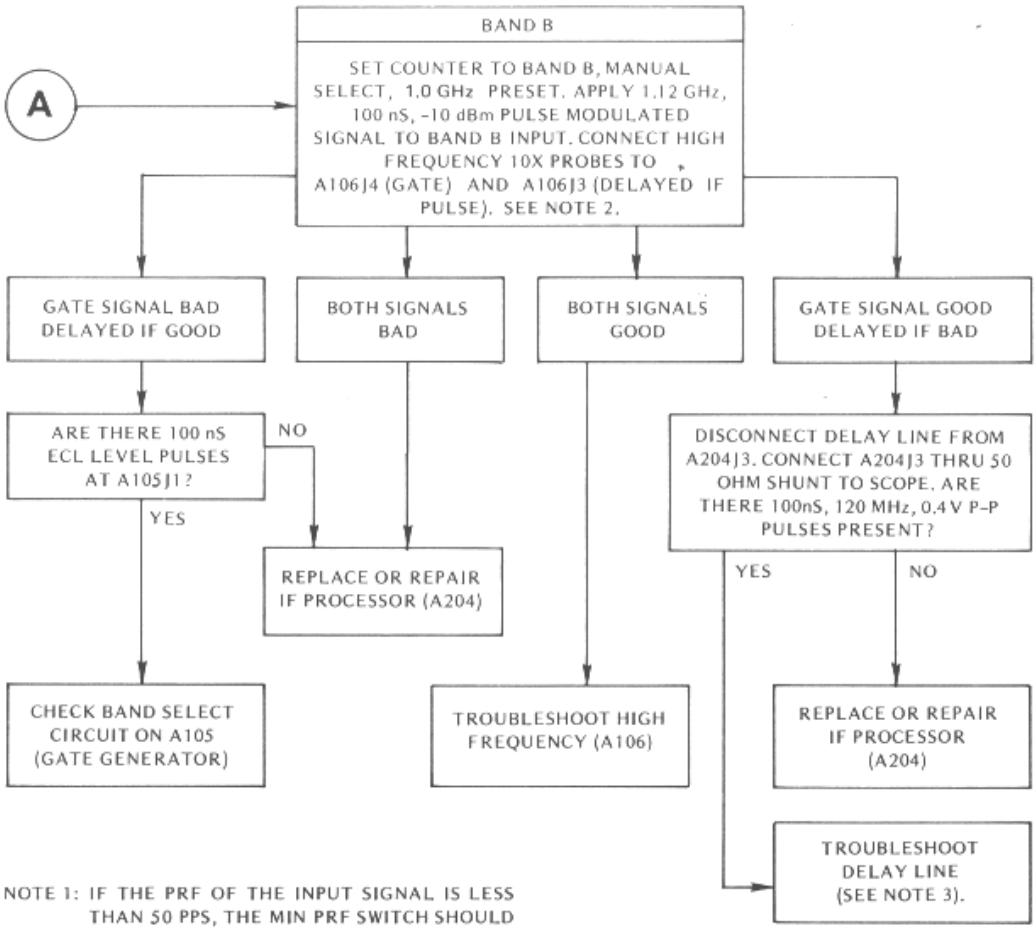


Figure 5-10. Pulse Input



NOTE 1: IF THE PRF OF THE INPUT SIGNAL IS LESS THAN 50 PPS, THE MIN PRF SWITCH SHOULD BE IN THE 0 Hz POSITION.

NOTE 2: IN ORDER TO MEASURE THE TRUE TIME RELATIONSHIP BETWEEN THE GATE AND DELAYED IF SIGNALS, IT WILL BE NECESSARY TO TAKE INTO CONSIDERATION THE DIFFERENCE IN TIME DELAY BETWEEN THE TWO CHANNELS OF THE OSCILLOSCOPE. REFER TO FIGURE 5-10A FOR WAVEFORMS, AND FIGURE 3-6 FOR TIMING DELAYS.

NOTE 3: DELAY LINE SPECIFICATIONS: IMPEDANCE: 50 OHMS. DELAY: 70 nS. ATTENUATION AT 100 MHz: 7 dB, AT 300 MHz: 13 dB. COUNTERS EQUIPPED WITH OPTION P2 (PRESCALER) HAVE TWO IDENTICAL DELAY LINES CONTAINED WITHIN ONE ASSEMBLY.

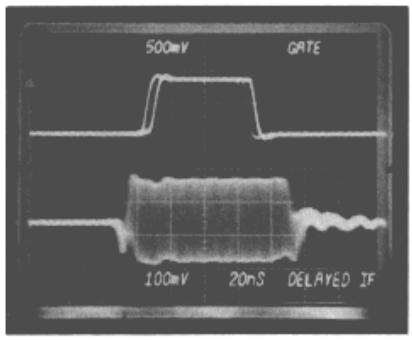


FIGURE 5-10A
DELAYED IF AND GATE SIGNALS

Figure 5-10. Pulse Input
(Continued)

Section 6
Adjustments and Calibrations

GENERAL

This section describes the procedures to be followed to correctly adjust the 451 Counter. In general, adjustments should only be made if the instrument is not operating within specifications, or following replacement of components. Recommended test equipment is specified on page 5-10. If adjustments do not result in specified performance, refer to Section 5.

GENERATING AND MEASURING NARROW RF PULSES

There are two potential problem areas that arise when generating narrow RF pulses by modulation of a CW source: (1) frequency pulling due to impedance changes in the modulator, and (2) video leakage of the modulating waveform.

The input impedance of a modulator generally varies with its state: on, off, or switching. This variation in loading will cause shifts in the frequency of the microwave source. The extent of this pulling effect is dependent upon the type of source, type of modulator, and the degree of isolation between them. Pulling of several megahertz for poorly isolated sources is not uncommon.

Modulators generally incorporate some form of fast switching diode, whose state is changed by the application of an appropriate bias current or voltage waveform. Coupling capacitors are used to separate the bias lines from the RF circuit. Video leakage is the transient signal caused by the modulating waveform being coupled into the RF lines. Usually this appears as a spike or ringing waveform at the leading and trailing edges of the modulating pulse. If care is not taken to provide adequate filtering, or otherwise eliminate this effect, significant measurement errors can occur, especially for fast rising pulses (less than 10 nanoseconds). On an unfiltered system, video leakage can exceed applied RF signals by several orders of magnitude.

In order to measure the peak power of an RF pulse, it will be necessary to use a calibrated crystal detector (such as the HP 8472A), a 50 ohm shunt feedthru to terminate the detector output, and a 50 MHz oscilloscope to observe the detected video pulse. The measurement is made by connecting the detector to the cable that normally feeds through the shunt to the scope. The observed peak amplitude of the pulse is then compared to the calibration curve of the detector to find the peak pulse power. The 3 dB pulse width is the time interval between the points on the pulse waveform corresponding to one-half the peak power.

IMPORTANT

Many adjustments are dependent upon previous ones. It is essential that care be taken to perform adjustments in exactly the order presented in the following procedure. Adjustment locations are shown in Figure 6-1.

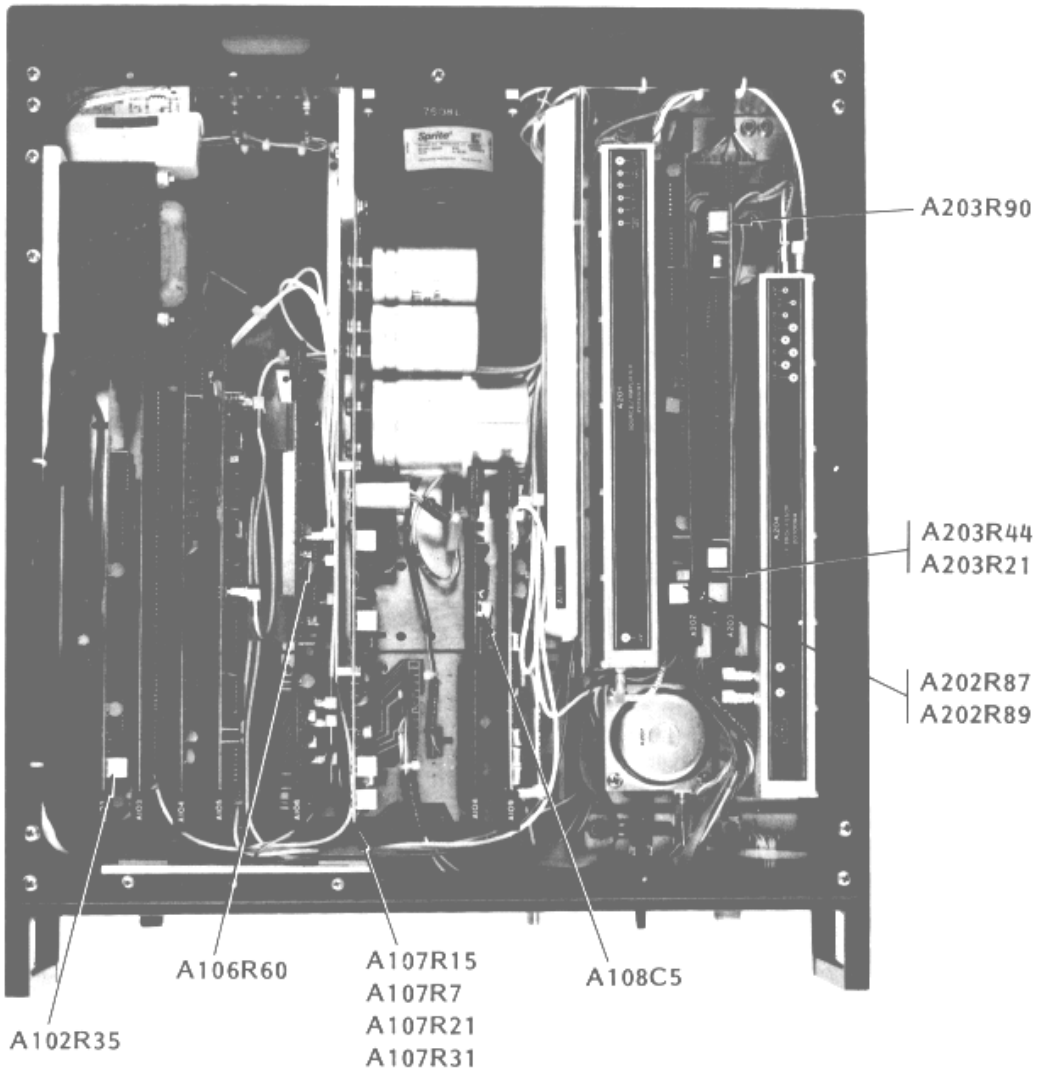


Figure 6-1. Calibration Adjustment Locator

POWER SUPPLY ADJUSTMENT

Prior to any power supply adjustment, the instrument should be allowed to warm-up for at least 20 minutes. All voltages are measured on Counter Interconnect board at A100P3. Adjust basic DC voltages as follows:

1. Connect DVM to ground at A100P3 pin 12.
2. Measure +12 VDC output at A100P3 pin 11. Adjust A107R7 until output is +12.000 ± .010 VDC.
3. Measure +5 VDC output at A100P3 pin 9. Adjust A107R15 until output is +5.000 ± .010 VDC.
4. Measure -12 VDC output at A100P3 pin 8. Adjust A107R21 until output is -12.000 ± .010 VDC.
5. Measure -5.2 VDC output at A103P3 pin 10. Adjust A107R31 until output is -5.200 ± .010 VDC.

TIME BASE CALIBRATION

IMPORTANT

The precision of time base calibration directly affects overall counter accuracy. Reasons for recalibration, and procedures to be used, should be thoroughly understood before attempting any readjustment.

The fractional frequency error in the frequency indicated by the counter, is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\Delta f_s}{f_s} = -\frac{\Delta f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus the inaccuracy associated with a frequency measurement is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

RTO CALIBRATION

1. Measure the frequency of the RTO (Room Temperature Crystal Oscillator) at the rear panel 10 MHz OUT connector with a second counter of known accuracy.
2. Adjust the RTO (if necessary) by turning A108C5 until the measured frequency is 10 000 000 ± 5 Hz.

TCXO CALIBRATION (OPTION P1)

Option P1 consists of a temperature compensated crystal oscillator (TCXO) mounted in place of the RTO on Oscillator board A108. The highest and lowest actual measured TCXO frequencies will differ by no more than 2 parts in 10^6 if the temperature is varied slowly from 0° to +50°C. Therefore, an indicated measurement will exhibit the same fluctuation even though the signal being measured is not changing.

To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side, the frequency to which it must be set at +25° C.

At approximate room temperature (+25° C), the slope of the frequency vs. temperature curve, is normally no worse than -1 X 10^{-7} parts per°C. Therefore, if the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10 000 000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5° C will result in a measured signal error due to oscillator temperature characteristics of no more than ± 2.5 X 10^{-7} parts.

Another source of inaccuracy in the measured signal due to the Time Base Oscillator originates in the natural aging characteristic of the crystal. Aging refers to the long term, irreversible change in frequency, generally in the positive direction, which all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is specified to be less than 3 X 10^{-7} parts per month. This may be expected to improve in time to be no worse than 1 X 10^{-6} parts per year in continuous service.

Error due to aging adds directly to error due to temperature perturbations. Thus the frequency of recalibration is dependent upon the overall accuracy requirement of the counter and its environment. For example: If the counter is subjected to the full operating temperature range and initially adjusted properly, then one month later the inaccuracy over temperature could be expected to vary from + 1.3 X 10^{-6} parts, to - 0.7 X 10^{-6} parts.

TCXO CALIBRATION PROCEDURE

1. Remove top cover of counter. Connect counter to a reliable power source (No voltage change). Note ambient temperature.

2. Measure the frequency of the TCXO at the rear panel 10 MHz OUT connector with a second counter of known calibration accuracy.

3. Adjust the TCXO (if necessary) by turning the calibration screw on the TCXO case until the measured frequency is the same as that shown on the TCXO calibration label (e.g. if + 2.6 shown on label set frequency to 10000003 Hz).

BAND A ADJUSTMENTS (Option P2)

If the High Frequency board (A106) is repaired or replaced, perform the adjustments given for high frequency (A106). No other Band A adjustment is required.

BAND B ADJUSTMENTS

CLOCK ADJUSTMENT, 40 kHz

NOTE: Required only upon replacement of YIG Comb Generator (A207), or Converter Sequencer board (A203).

1. Set counter to Band B, MANUAL SELECT, and 01.0 GHz PRESET FREQUENCY.
2. Jumper A202TP1 to A202TP3. Ground A202TP5.
3. Connect oscilloscope Channel A to A202U1 pin 9, and Channel B to A202U1 pin 4.
4. Adjust A202R89 for a symmetrical waveform as shown in the upper trace of Figure 6-2. (All pulses in the train should be of equal duration.)

If necessary, select a new value for A203R93 so the leading and trailing edges of the 20 kHz reference (lower trace) occur in the center of the detected modulation pulses. (If A203R93 is changed, re-adjust A202R89 as stated in (4) above.)

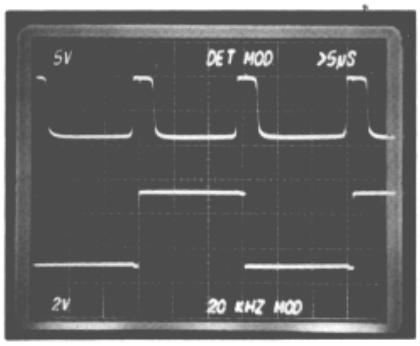


Figure 6-2. Detected Mod/20 kHz Reference Pulse Timing

SLOPE AND OFFSET ADJUSTMENT

1. Repeat Band B adjustments 1 through 4.

2. Change preset in 1 GHz steps from 1 to 18 GHz, adjusting A202R87 to produce a symmetrical waveform across the band.

3. Repeat steps 1 and 2 above as necessary.

4. Remove jumper from A202TP1 and A202TP3. Remove ground from A202TP5.

ATTENUATOR DRIVER ADJUSTMENT

NOTE 1:
These adjustments are difficult to make, and require careful set-up by personnel familiar with microwave return loss measurements. These adjustments affect only the Band B input VSWR of the counter, and should be made only: (1) when it is known that there is excessive input VSWR, (2) the attenuator driver on A203 has been repaired, or (3) if A203 or A206 have been replaced.

NOTE 2:
To make a meaningful return loss measurement, use a directional coupler with a minimum directivity of at least 25 dB (Example: Hp 779D).

1. Set counter to Band B, AUTO SWEEP, 00.0 GHz START FREQUENCY.

2. Carefully set-up equipment as shown in Figure 6-3. Note especially where cables or adapters must not be used (which would degrade accuracy of the adjustment).

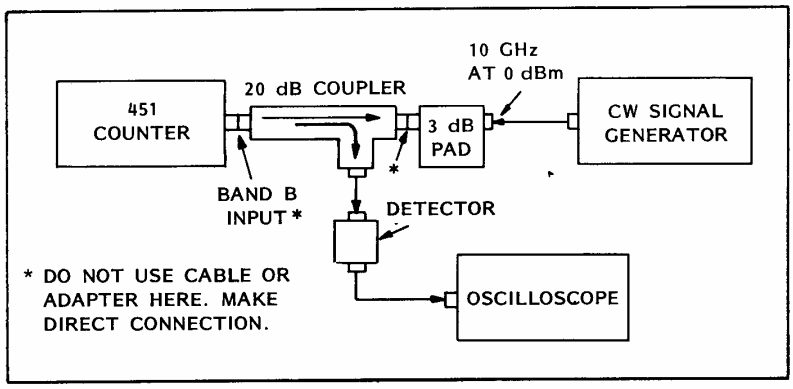


Figure 6-3. Return Loss Measurement Set-Up

3. Set Limiter/Attenuator (A206) to maximum insertion loss, by connecting a jumper between A203-TP16 and TP21.

4. Adjust A203R44 for maximum return loss (waveform will be a DC level).

NOTE 3:
As R44 is rotated from full ccw to full cw, the amplitude observed on the scope will go from a maximum point through a minimum point and then to a maximum again. Maximum return loss (minimum reflected signal) occurs at the minimum point.

5. Remove jumper from A203TP16 to TP21.

6. Cycle Limiter/Attenuator (A206) through its normal operating range by removing and grounding the cable to A204J4.

7. Inhibit the counter from locking up by jumpering A203TP14 to TP16.

8. Connect an 0.47uf capacitor across A203C2.

9. Trigger scope from A203TP17 (Attenuator Control Ramp). See Note 4.

10. Adjust A203R21 for maximum return loss. See Note 3, and Figure 6-4 for typical waveform.

11. Remove jumper between A203TP14 and TP16. Remove capacitor. Reconnect cable to A204J4.

NOTE 4:
If a 0 to +1 Volt ramp is not present at TP17, momentarily disconnect the jumper from A203TP14 to A203PT16 and reconnect the jumper.

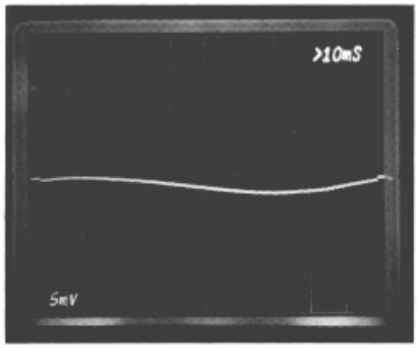


Figure 6-4. Return Loss Measurement

ATTENUATOR CONTROL ADJUSTMENT

NOTE:
To be performed only upon installation of a new Limiter/Attenuator (A206), or replacement of the Converter Sequencer board (A203).

1. Connect an 0.47uf capacitor across A203C2.

2. Connect the Channel A 10X probe of scope to A203J1 pin 1 (I_{series}). Connect Channel B 10X probe to A203TP17.

3. Remove and ground cable to A204J4.

4. Connect jumper between A203TP14 and TP16.

5. Select a value for A203R18 so the first two or three steps of the Attenuator Control Ramp have no effect upon I_{series} (see Figure 6-5).

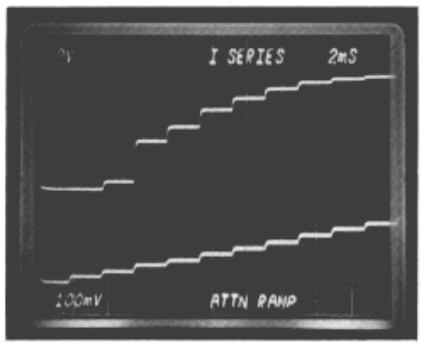


Figure 6-5. Attenuator Control Ramp Offset Adjustment

6. Remove jumper between A203TP14 and TP16. Remove capacitor. Reconnect cable to A204J4.

7. Apply a 0 dBm, 1.4 GHz CW signal to Band B input.

8. Press RESET switch. Increase signal level to the Band B input until the REDUCE SIGNAL light comes on. (Light should come on between +4 and +6 dBm. If it does not, select a new value for A203R17, and repeat steps 7 and 8 until it does.)

COMB LEVELING ADJUSTMENT

1. Set-up counter as described in Attenuator Drive Adjustment, step 1.

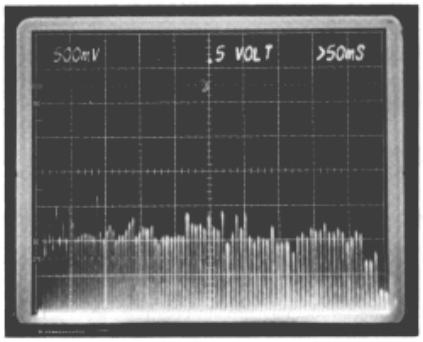
2. Jumper A203TP14, TP15, and TP16 together.

3. Connect Channel A 10X scope probe to A203TP12. Trigger scope from A203TP20 (Reset).

4. Press RESET switch.

5. Adjust A203R90 to level comb lines to 1 volt nominal (see Figure 6-6).

6. Remove jumpers from TP14, TP15, and TP16.



< 50 msec, .5V/div., Comb Level

Figure 6-6. Comb Leveling

HIGH FREQUENCY ADJUSTMENT, A106

GATE ACCURACY, BAND A (Option P2)

1. Set-up counter and perform error measurement as described in Section 7.

2. Adjust A106R60 to minimize difference between averaged pulse reading and CW reading.

NOTE:
If using Method A, it will be necessary to (a) have a stable RF source that will not be pulled more than 10 kHz while being modulated by a 100 nS pulse, (b) have no video information on the RF pulse, and (c) have a means of measuring RF pulse width and amplitude. Also, when using Method A, adjust A106-R60 so the average pulse reading is centered about the CW reading (gate error equal to zero).

3. Gate Accuracy – for counters NOT equipped with Band A (Option P2):
   A. Set SAMPLE RATE control fully counter-clock-wise, BAND SELECT to Band B, MANUAL SELECT, and 1.0 PRESET FREQUENCY.

   B. Apply a 1.3 GHz CW signal at -10 dBm to the Band B input.

   C. Adjust A106R60 per step 2.

Section 7
Performance Tests

GENERAL

This section contains the information the user will need to verify that the counter meets specifications over the entire frequency range, with both CW and pulse inputs.

NOTE: For the verification to specifications not included in this section please consult the factory.

VARIABLE LINE VOLTAGE

During the performance tests the counter should be connected to the power source through a variable voltage device so that the line voltage can be varied ± 10% from nominal (100/120 or 220/240 VAC), to assure proper operation of the counter under various supply conditions.

TEST EQUIPMENT

Please refer to Section 5 for a list of the test equipment that is recommended. Other equipment may be used provided that its performance is equal to, or better than, that listed.

PERFORMANCE TESTS

RANGE, SENSITIVITY, AND MINIMUM PULSE WIDTH – BAND A

1. Set SAMPLE RATE control fully counter clockwise, and set BAND SELECT switch to Band A.
2. Connect a CW signal source to the Band A input.
3. Vary the source frequency from 300 MHz to 950 MHz at -10 dBm. Display should show the correct frequency.
4. Connect a 100 nsec pulse modulated signal to the Band A input. Set level to -10 dBm. Vary the source frequency from 300 MHz to 950 MHz. Display should show correct frequency.

NOTE: Refer to Section 6 for pulse width measurement.

RANGE, SENSITIVITY, AND MINIMUM PULSE WIDTH – BAND B

1. Set SAMPLE RATE control fully counter clockwise, and set BAND SELECT switch to Band B, AUTO SWEEP, and 00.0 GHz START FREQUENCY.
2. Connect a CW leveled source to the Band B input.
3. Vary the source frequency from 925 MHz to 18 GHz at each of the following levels.
   925 MHz to 10 GHz, -10 dBm and 10 GHz to 18 GHz, -5 dBm
4. Connect a 100 nsec pulse modulated signal to the Band B input. Repeat step 3. See Section 6 for pulse width measurement.

GATE ERROR – BAND A

Refer to Section 3 for description of gate error.

1. Set SAMPLE RATE control fully counter clockwise, and set BAND SELECT switch to Band A.
2. Apply a 950 MHz CW signal at -10 dBm to the Band A input.

Gate error readings can be taken using two modulation methods and two measurement methods.

MODULATION METHOD

1. Pulse modulate signal source with 100 nsec wide pulse.
2. Simulate modulation by applying 100 nsec wide ENABLE pulses to input inhibit connector on the rear panel. This method is preferred. It avoids errors associated with possible pulling of the signal source.

ERROR MEASUREMENT USING STRIP CHART RECORDER

1. Set up test equipment as shown in Figure 3-7, with recorder connected to the BCD output of the counter.
2. Record the CW frequency reading.
3. Pulse modulate using method 1 or 2.
4. Record the average pulse reading.
5. Gate error is equal to the difference between the reading for step 2 and 4. For 100 n sec wide pulses, error should be less than 1.42 MHz.

ERROR MEASUREMENT USING SCRATCH PAD

1. Reduce SAMPLE RATE time so each reading can be recorded on scratch pad or chart.
2. Record CW frequency reading.
3. Pulse modulate using method 1 or 2.
4. Record and then average ten or more successive readings.
5. Gate error is equal to the difference between the readings for step 2 and 4. For 100 n sec wide pulses, error should be less than 1.42 MHz.

GATE ERROR – BAND B

Refer to Section 3 for description of gate error.

1. Set SAMPLE RATE control fully counter clockwise, set BAND SELECT to Band B, MANUAL SWEEP, and 1.0 GHz start frequency.
2. Apply a 1.3 GHz CW signal at -10 dBm to the Band B input.
3. Repeat Gate Error Measurement step 3. Gate error should be less than 570 kHz. Note that the Gate Error is a function of IF frequency.

REAR PANEL OUTPUT LEVELS

1. Apply a pulse modulated signal to the counter.

2. Measure GATE and SIGNAL THRESHOLD outputs using a 50 ohm shunt feedthru to an oscilloscope.

Gate output should be at least -0.5 VDC, corresponding to counter gate. The signal threshold output should be zero VDC with no RF signal, and at least -0.5 VDC when RF is present.

REAR PANEL INPUT INHIBIT LEVELS

The input inhibit has a 50 ohm source impedance returned to -2.0 VDC.

1. Apply a CW signal to the counter.

2. Apply -1.7 VDC to the input inhibit connector. Counter should operate normally.

3. Apply -0.9 VDC to the input inhibit connector. Counter should stop counting, and operate as if a no signal condition existed.

Section 8
Functional Description and Illustrated Parts Breakdown

This section contains a functional description, a parts list, an illustration and a schematic for each printed circuit board used in this counter.

The parts list is broken down by types of components, listed in alphanumeric sequence. The components that have a different reference designator (REF DES), but have the same EIP part number, are described for the first such component listed. Subsequent descriptions of that component will refer to the first entry. The total number of like components used on the same assembly will be listed with the first entry. in the column identified as UNITS PER ASSY.

The last two columns of the parts list will supply the manufacturer part number and their Federal Supply Code for Manufacturers (FSCM) number. A list of manufacturers names, addresses and their FSCM is given in Appendix A. The FSCM number is used as a guide to the maker or supplier of a part.

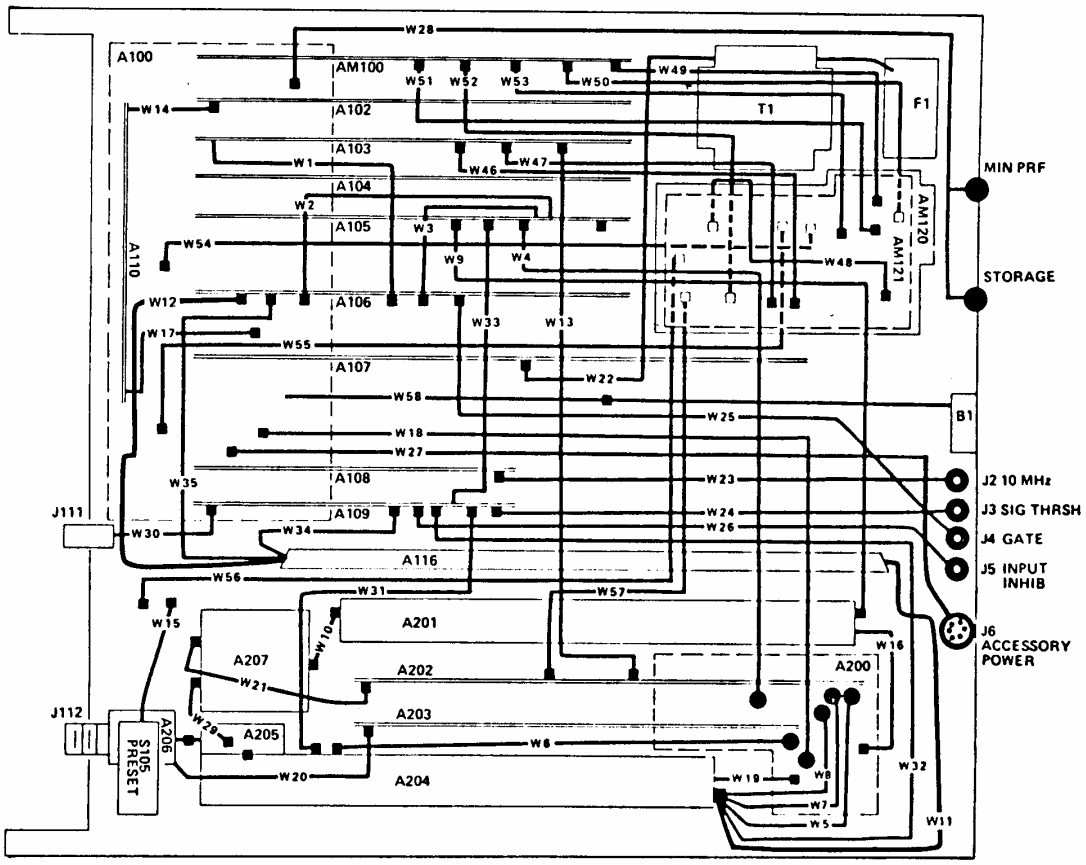
Pages 8-3 through 8-5 contain the top assembly of the counter and other basic information. After page 8-8 you will note that the page numbers have a three digit first number followed by a dashed number. The three digit number reflects the number of the assembly being described on those pages. The dashed number is the page sequence for that assembly description. For example, pages 105-1 through 105-7 all relate to the A105 printed circuit board. This page numbering system facilitates simple, modular page replacement when an assembly revision makes a manual update necessary.

REFERENCE DESIGNATORS

A	Assembly
B	Battery or Fan
C	Capacitor
CR	Diode
DS	Indicator (display)
F	Fuse
J	Jack or Connector
K	Relay
L	Inductor
P	Plug or PCB contacts
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
U	Integrated Circuit
W	Wire (cable)
X	Socket or Holder
Q1-3	Q1 through Q3
Q1/2	Q1 and Q2 (matched pair)

ABBREVIATIONS

CAP	Capacitor
CBN	Carbon
CER	Ceramic
CMT	Cermet
CNTR	Counter
CONV	Converter
COMP	Composition
CONN	Connector
DI	Diode
ELEC	Electrolytic
FDTH	Feedthrough
FLM	Film
FML	Female
GP	General Purpose
IC	Integrated Circuit
K	Kilo (x 1,000)
LED	Light-emitting-diode
M	Meg (x 1,000,000)
MET OX	Metal Oxide
MF	Metal Film
MH	Millihenry
ML	Male
MTCH PR	Matched Pair
PC	Printed Circuit
PCB	PC Board Assembly
PF	Picofarad
PREC	Precision
RSTR	Resistor
RT AN	Right Angle
S.A.T.	Value or type selected during factory test. Part may not be used.
SW	Switch
TANT	Tantalum
TRIM	Trimmer
UF	Microfarad
UH	Microhenry
VAR	Variable
WPRF	Waterproof
WW	Wirewound
XSTR	Transistor



INCLUDES OPTIONS P1, P2, AND P5

Figure 8-1. Assembly Locator and Cable Interconnection

451 MICROWAVE PULSE COUNTER

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	Counter, 451	2010070			
–1	Front Panel Assy	2010072	1	EIP	
	Overlay	5210128	1	EIP	
	Sub Panel	5210089	1	EIP	
	Window, Red Acrylic	5220016	1	EIP	
	Power Switch	4500008	1	EIP	
	Knob, Sample Rate	5000056	1	RB67-OML .25 SHFT	86797
	MAN/AUTO Switch	4510007	1	83045SQ	04009
	Signal Lamp, 5V, 15mA, Red	2800010	1	2L5S-RT PFL 5/15	08717
	Thumbwheel Switch, BCD	4540002	1	900048	23880
–2	Rear Panel Assy	2010075	1	EIP	
	Overlay	5210142	1	EIP	
J1	F1/Power Module	2650003	1	EIP	
J2	Conn, BNC, 10 MHz	2610024	1		
J3	(P103) Coax Assy, Signal Thresh.	2040086	1	EIP (W24)	
J4	(P104) Coax Assy, Gate	2040087	1	EIP (W25)	
J5	(P105) Coax Assy, Input Inhibit	2040088	1	EIP (W26)	
J6	Conn, 6 pin, PWR Out	2640022	1	RA 1.306NYL	
J7	(P1) Remote Prog/BCD, Opt P4	2020082	1	R/O Option P4	
S102	Switch, Min Prf. (0-50 Hz)	4510001	1	7101H	09353
S103	Switch, Storage ON/OFF	4510001	1	7101H	09353
B1	Fan	5000151	1	760/126LF/182/1115	
T1	Transformer	4900004	1	EIP	
–3	Tilt Bail	5000055	1	453458	21793
–4	Top Cover	5210023	1	EIP	
–5	Bottom Cover	5210024	1	EIP	
–6	MTG foot	5220003	4	453457	21793
–7	Power Cord, Domestic	5440002	1	17250	70903
	Power Cord, Export	5440017	1		
–8	Delay Line Assy (AH2)	2010081	1		

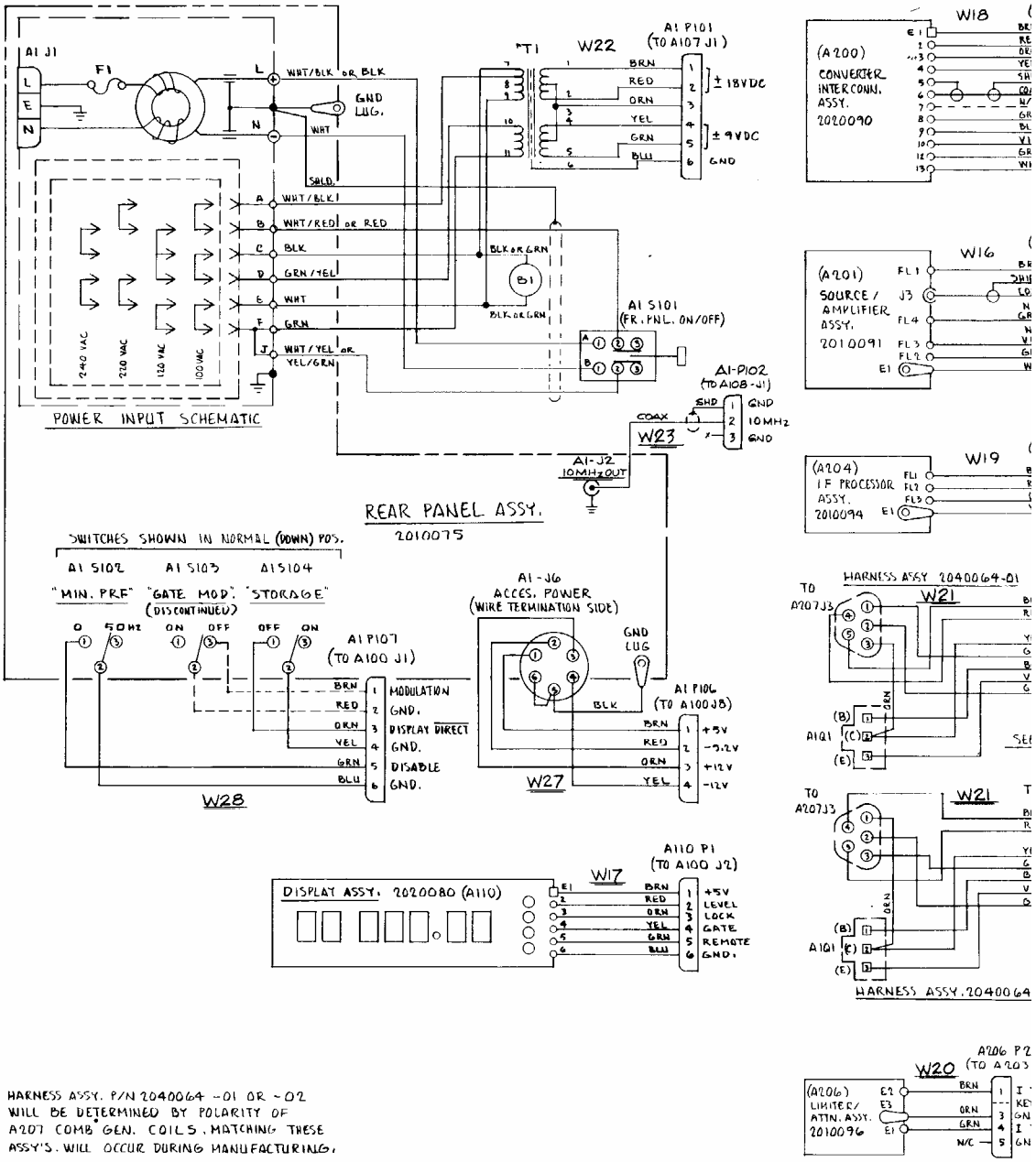
451 MICROWAVE PULSE COUNTER

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
	PCB Assemblies				
A100	Counter Interconnect	2020070	1	100-1 (Page)	
A102	Count Chain Control	2020084	1	102-1	
A103	Count Chain	2020083	1	103-1	
A104	Control	2020074	1	104-1	
A105	Gate Generator	2020085	1	105-1	
A106	High Frequency	2020081	1	106-1	
A107	Power Supply	2020077	1	107-1	
A108	Reference Oscillator Buffer	2020078	1	108-1	
A109	Prescaler (Option P2)	2020079	Ref	P2-1	
A110	Display	2020080	1	110-1	
A111	BCD/Remote (Option P4)	2020082	Ref	P4-1	
A200	Converter Interconnect	2020090	1	200-1	
A201	Source Amplifier	2020091	1	201-1	
A202	YIG Control	2020092	1	202-1	
A203	Converter Sequencer	2020093	1	203-1	
A204	IF Processor	2020094	1	204-1	
A205	Mixer	2010007-02	1	Not shown (No replaceable parts)	
A206	Limiter/Attenuator	2010113	1	Not shown (No replaceable parts)	
A207	Yig Comb Generator	2010097-02	1	Not shown (No replaceable parts)	
AM100	Microprocessor, GPIB (Option P5)	2020060-02	Ref	P5-17	
AM120	BCD Output, GPIB (Option P5)	2020086	Ref	P5-25	
AM121	Remote/Local, GPIB (Option P5)	2020087	Ref	P5-31	
	CABLES				
W1	A103 P2 to A106 J5	2040110			
W2	A105 P2 to A106 J1	2040091			
W3	A105 P3 to A106 J4	2040092			
W4	A200 P2 to A105 J1	2040095			
W5	A200 P3 to A204 J6	2040096			
W6	A200 P4 to A204 J2	2040097			
W7	A200 P5 to A204 J7	2040098			
W8	A200 P6 to A204 J4	2040099			
W9	A201 J1 to A105 J4	2040085			
W10	A201 J2 to A207 J2	2040094			
W11	A112 P1 to A204 J3	2040093			
W12	A112 P2 to A106 J3	2040093			
W13	A103 J3 to A202 J2	2040074			
W14	A110 P2 to A102 J1	2040073			
W15	A1-P121 to A202 J1				
W16	A201 P1 to A200 J2	2040112			
W17	A110 P1 to A100 J2	2040063-01			
W18	A200 P1 to A100 J3	2040068			
W19	A204 P1 to A200 J1	2040066			
W20	A206 P2 to A203 J1	2040065			
W21	A202 J3 to A1 Q1 and A107 J3	2040064			
W22	A1 (T1) P101 to A107 J1				

451 MICROWAVE PULSE COUNTER

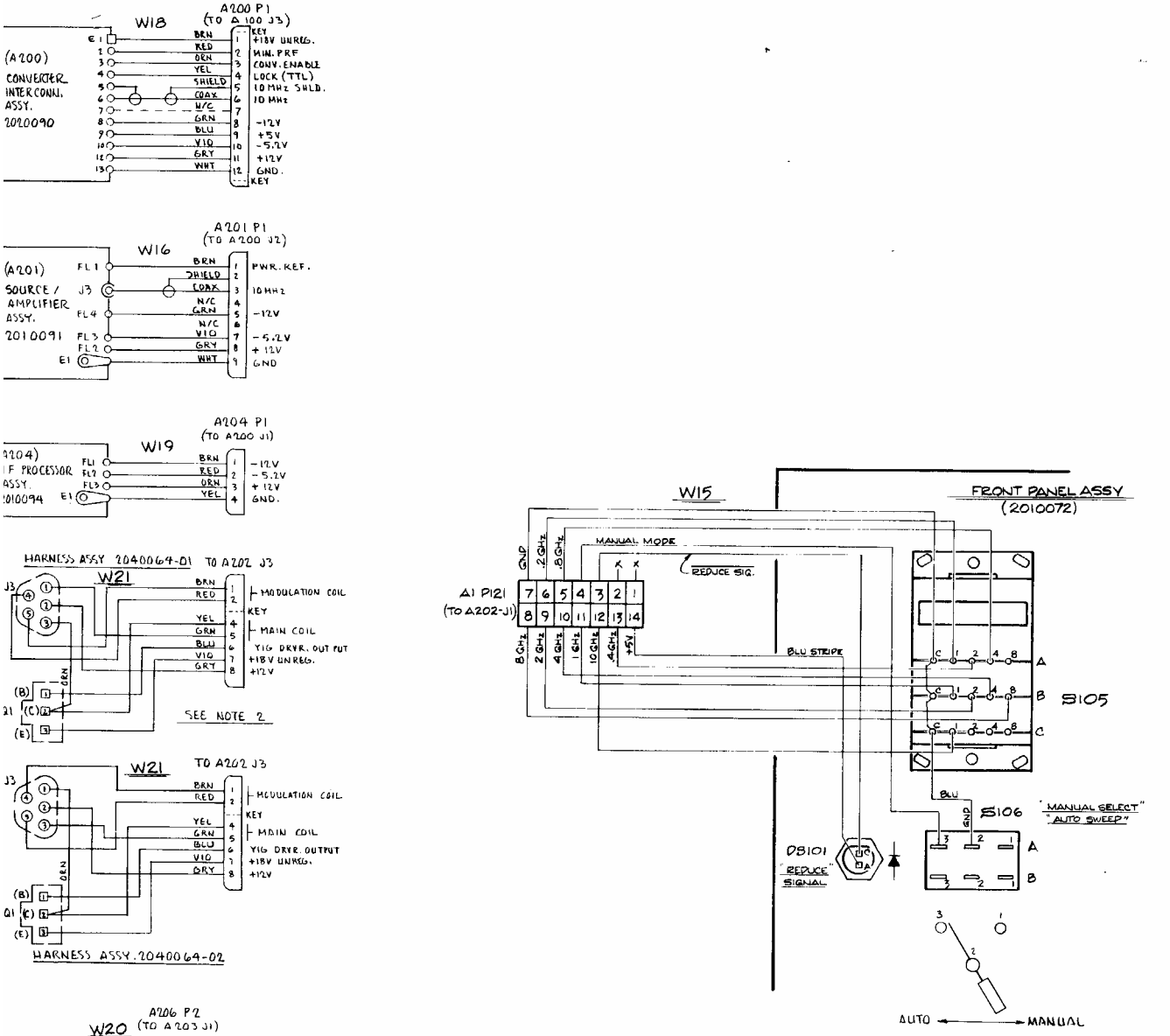
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
W23	A1 (J2) P102 to A108 J1				
W24	A1 (J3) P103 to A204 J1	2040086			
W25	A1 (J4) P104 to A106 J6	2040087			
W26	A1 (J5) P105 to A204 J5	2040088			
W27	A1 (J6) P106 to A100 J8				
W28	A1 P107 to A100 J1				
W29	A205 P1 to A207 J1	2040089			
	CABLES, OPTION P2				
W24	A1 P103 to A109 J6	2040108			
W26	A1 P105 to A109 J3	2040109			
W30	A1 J111 to A109 J1	2040102			
W31	A204 J1 to A109 J5	2040103			
W32	A204 J5 to A109 J4	2040104			
W33	A105 J2 to A109 P2	2040107			
W34	A116 P1 to A109 J2	2040101			
W35	A116 P2 to A106 J2	2040101			
A116	Dual Delay Line	2010086			
W	Cable, Prescaler Delay	2040101			
	CABLES, OPTION P4				
W15	A1 P121 to A100 J6				
W40	A111 J1 to A100 J4	2040075			
W41	A111 J2 to A100 J5	2040076			
W42	A111 J4 to A202 J1	2040077			
W43	A111 J5 to A103 J5	2040078			
W44	A111 J6 to A103 J1	2040079			
W45	Same as W44				
	CABLES, OPTION P5				
W48	AM120J3 to AM121J2	2040138	1		
W49	AM120J4 to AM100J2	2040122-01			
W50	AM121J1 to AM100J3	2040122-01			
W51	AM100J6 to AM120J5	2040123-01			
W52	AM100J5 to AM121J5	2040123-01			
W53	AM120J6 to AM100J4	2040139			
W54	AM121J3 to A100J4	2040140			
W55	AM121J4 to A100J5	2040141			
W56	AM121J6 to A100J7	2040142			
W57	AM121J7 to A202J1	2040143			
W48	AM120J3 to AM121J2	2040138			

PAGE LEFT BLANK INTENTIONALLY



2. HARNESS ASSY. P/N 2040064 -01 OR -02 WILL BE DETERMINED BY POLARITY OF A207 COMB GEN. COILS. MATCHING THESE ASSY'S. WILL OCCUR DURING MANUFACTURING.

1. INFORMATION SHOWN ON THIS DRAWING DENOTES PIN ASSIGNMENTS FOR HARNESS ASSY'S ONLY. REFER TO CABLE CONN. GUIDE P/N 5560032, FOR COAX CABLE AND FLAT RIBBON CABLE INTERCONNECTION.



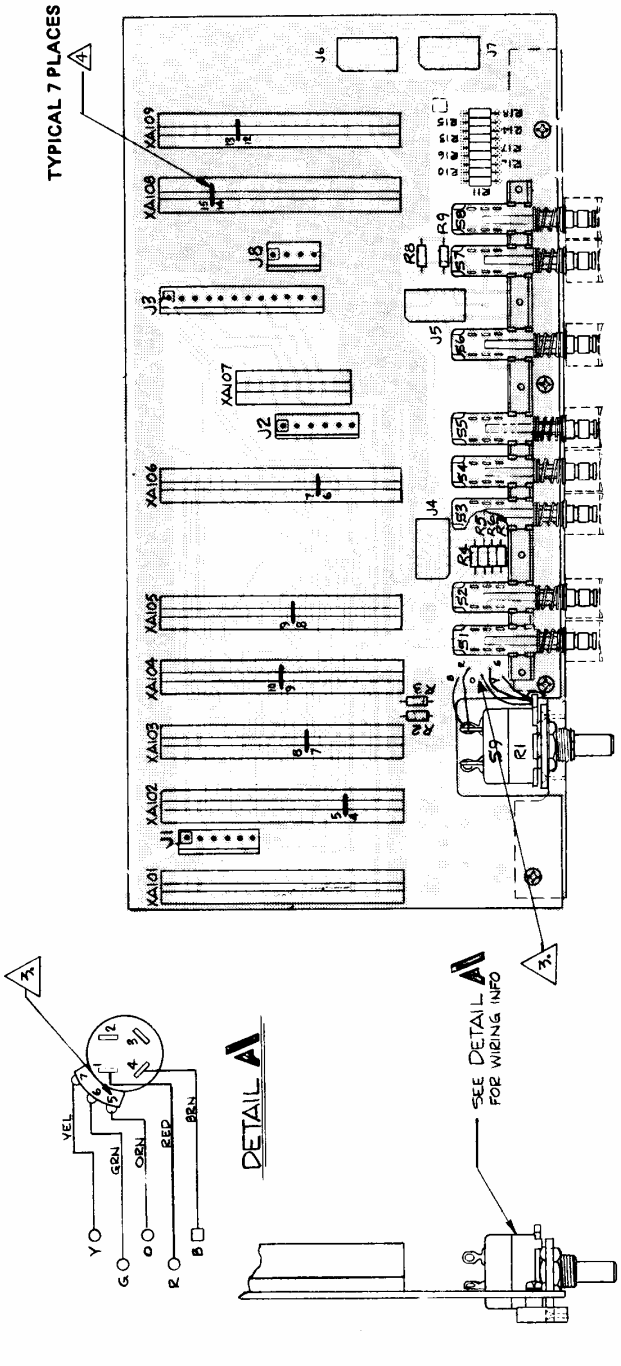
5520005 - A

Figure 8-2. Interconnection Diagram

A100 COUNTER INTERCONNECT

2020070 - P

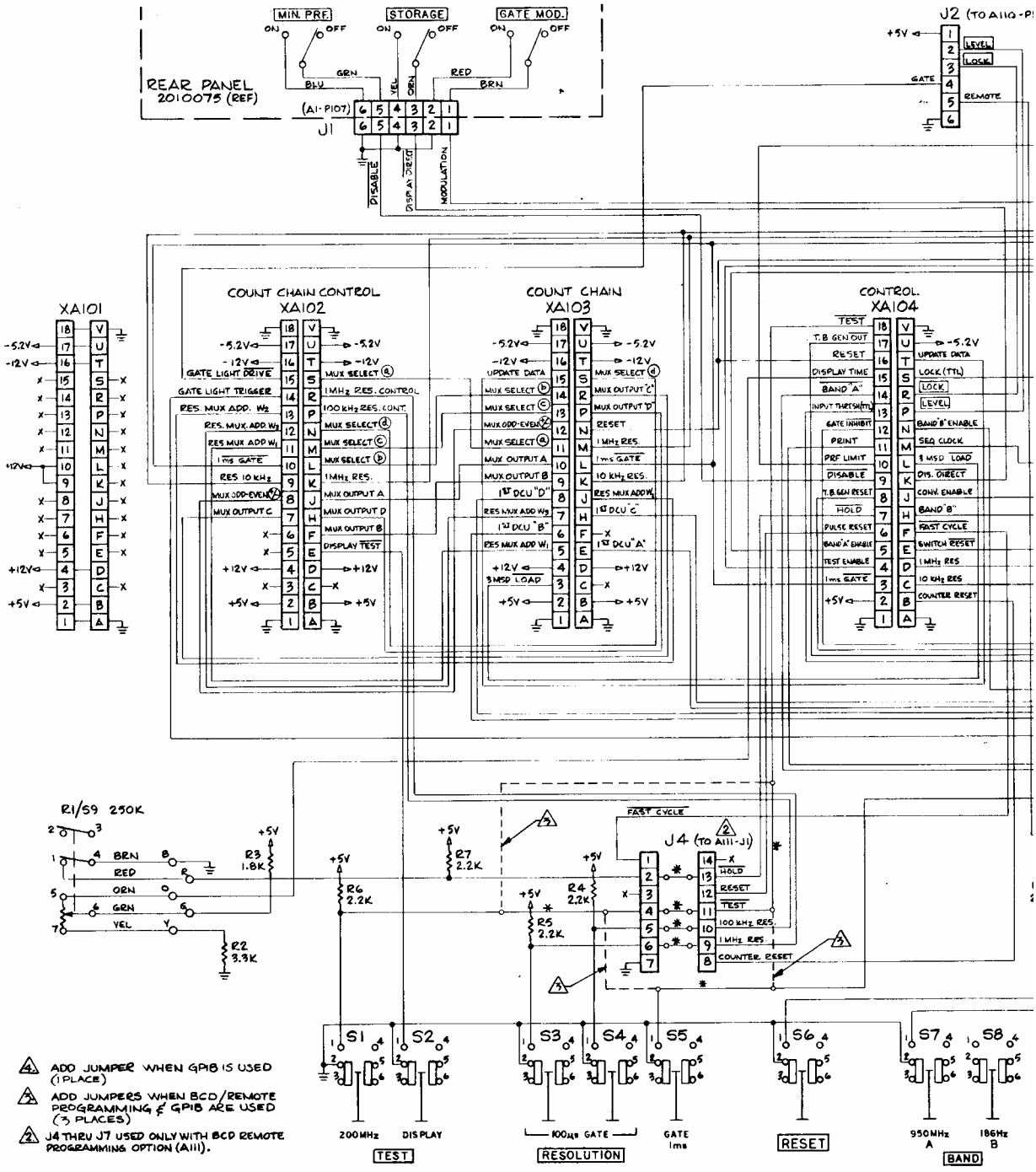
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A100	Counter Interconnect	2020070	1	EIP	34257
J1	PC Wafer, 6 pin	2620016	2	09-60-1061	
J2	J1				
J3	PC Wafer, 12 pin	2620044	1	09-60-1121	
J4	Socket, 14 pin	2630015	4	640357-1	02660
J5 thru J7	J4				
J8	PC Wafer, 4 pin	2620061	1	09-65-1041	
R1(S9)	Variable 250K (SPDT SW)	4290001	1	EF8078/RVF45	11237
R2	Comp, 3.3K, 5%, 1/4 W	4010332	1	RC07GF332J	81349
R3	Comp, 1.8K, 5%, 1/4 W	4010182	1	RC07GF182J	81349
R4	Comp, 2.2K, 5%, 1/4 W	4010222	15	RC07GF222J	81349
R5 thru R18	R4				
S1 thru S8	Switch, 8 station push button	4500010	1		
S9	See R1/S9				

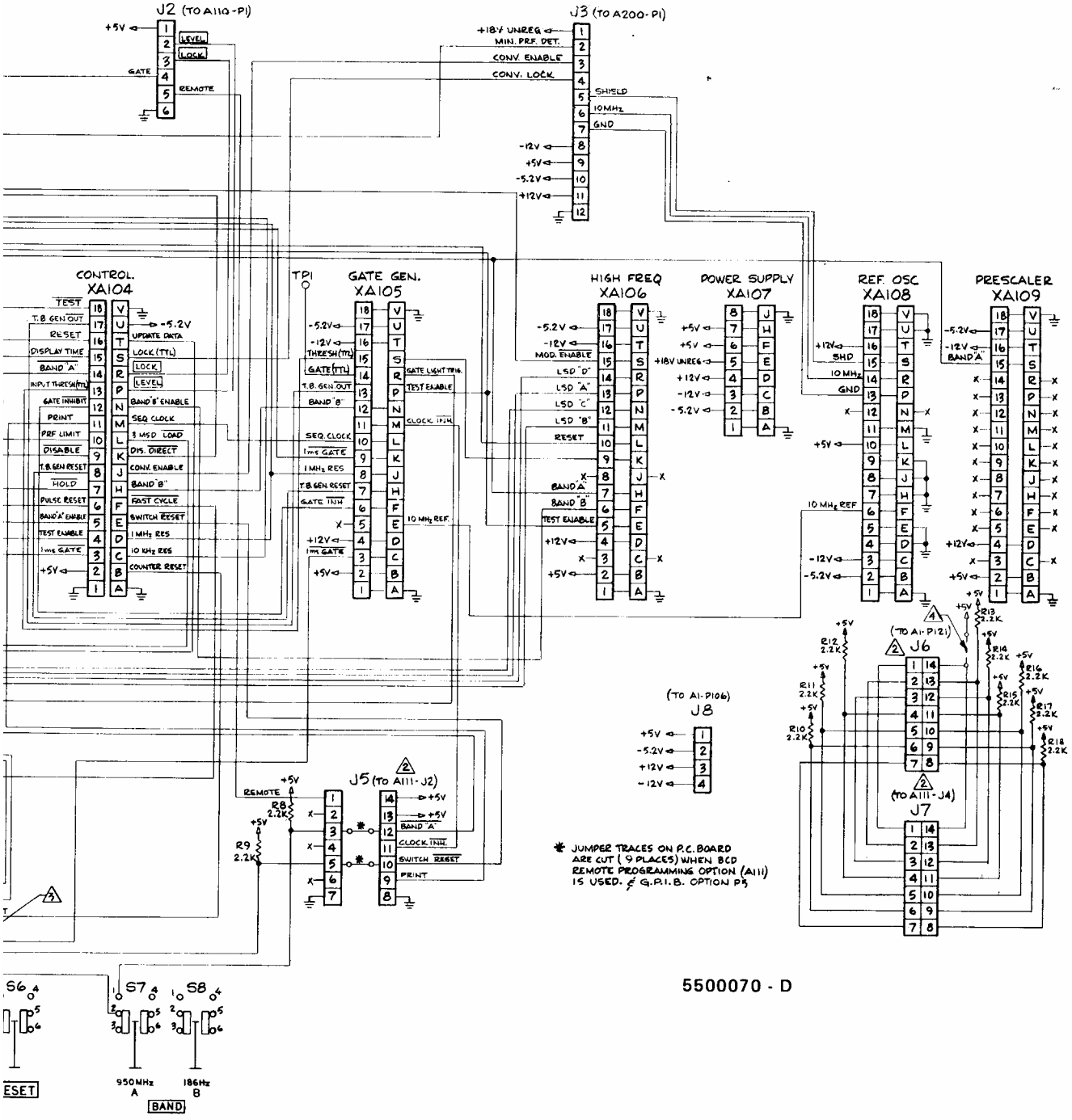


4 POLARIZING KEYS MUST BE CENTERED BETWEEN PINS IN CONNECTOR AND INSTALLED WITH CARE TO AVOID DAMAGE TO PINS. RECOMMEND USE OF AMP INSERTION TOOL P/N 91081-1.

3 SLEEVE TERMINAL R1/S1 - 5 (ORG)

Figure 100-1. Counter Interconnect Component Locator


REAR PANEL
2010075 (REF)
MIN. PRF.
STORAGE
GATE MOD.
ON
OFF
BLU
GRN
VEL
ORN
RED
BRN
(A1-P107)
J1
DISABLE
DISPLAY DIRECT
MODULATION
J2 (TO A11Q-P1)
+5V
LEVEL
LOCK
GATE
REMOTE
XA101
COUNT CHAIN CONTROL
XA102
COUNT CHAIN
XA103
CONTROL
XA104
-5.2V
-12V
+12V
+5V
GATE LIGHT DRIVE
GATE LIGHT TRIGGER
RES. MUX ADD. W2
RES. MUX ADD W3
RES MUX ADD W1
1ms GATE
RES 10 kHz
MUX ODD-EVEN
MUX OUTPUT C
MUX SELECT
1MHz RES. CONTROL
100 kHz RES. CONT.
1MHz RES.
MUX OUTPUT A
MUX OUTPUT D
MUX OUTPUT B
DISPLAY TEST
UPDATE DATA
MUX OUTPUT C
MUX OUTPUT D
RESET
1 MHz RES.
10 kHz RES.
1ST DCU "D"
1ST DCU "C"
1ST DCU "B"
1ST DCU "A"
3 MSD LOAD
TEST
T.B GEN OUT
DISPLAY TIME
BAND "A"
INPUT THRESH(TTL)
GATE INHIBIT
PRINT
PRF LIMIT
DISABLE
T.B GEN RESET
HOLD
PULSE RESET
BAND "A" ENABLE
TEST ENABLE
LOCK (TTL)
BAND "B" ENABLE
SEQ CLOCK
3 MSD LOAD
DIS. DIRECT
CONV. ENABLE
BAND "B"
FAST CYCLE
SWITCH RESET
1 MHz RES
10 kHz RES
COUNTER RESET
R1/S9 250K
R2 3.3K
R3 1.8K
R4 2.2K
R5 2.2K
R6 2.2K
R7 2.2K
J4 (TO A111-J1)
S1
S2
S3
S4
S5
S6
S7
S8
200MHz
DISPLAY
TEST
100μs GATE
RESOLUTION
GATE 1ms
RESET
950MHz A
186Hz B
BAND
4 ADD JUMPER WHEN GPIB IS USED (1 PLACE)
3 ADD JUMPERS WHEN BCD/REMOTE PROGRAMMING & GPIB ARE USED (3 PLACES)
2 J4 THRU J7 USED ONLY WITH BCD REMOTE PROGRAMMING OPTION (A111).



5500070 - D

Figure 100-2, Counter Interconnect Schematic

A102
COUNT CHAIN CONTROL
(2020084)

The Count Chain Control A102 controls and processes the flow of information on Count Chain board A103, and drives the front panel visual display. A pulse-stretcher and driver (on A102) also operate the GATE indicator on the front panel of the counter.

The clock generator, a ÷16 counter, and a 3-8 line decoder, serve to produce a sequence of eight addresses. These cause the DCU's on A103 to read out their BCD contents, in sequence, back to the data input of A102. The digits of the number representing the frequency measured by the counter are thus read in sequence into A102. The BCD numbers are decoded by U8 to drive the segments of each display digit on Display board A110. The same address generator that selected DCU's on A103, now addresses and drives the proper display digit of A110, so the number of a particular DCU of A103 will be displayed in the proper position. The address drive to certain display digits may be removed (to blank these digits) via the RESOLUTION switches.

The gate trigger is applied to a pulse-stretcher on A102. This insures that the gate control signal is of sufficient duration that the GATE indicator will produce a visible flash for each measurement cycle of the counter. (Short gates of 100 μs would not otherwise be visible.)

DISPLAY ADDRESS GENERATOR (U6, U9-11)

The Address Generator is driven by the clock generated in U6 at a 200 kHz rate. This drives binary counter U9, producing a sequence of sixteen different states on its four output lines. The last three lines: B, C, and D, drive decoder U10 which produces an output on one of eight output lines for each of the eight different states of the inputs: B, C, and D.

Seven of the eight single line outputs of decoder U10 are used to select display digits directly. The address to the DCU's of A103 however, is a one-of-four line code, plus an odd-even code on a fifth line. The one-of-four line code is obtained by combining successive outputs of decoder U10 in groups of two in the four AND gates of U11. The odd-even code is simply the A input to U10.

DISPLAY DECODER, DRIVER, AND LEADING ZERO SUPPRESSION CIRCUITS (U2, U4, U8)

The BCD to 7-segment decoder is included in U8. It directly supplies the cathode currents to the segments of the display digits which must be illuminated to display the number given by the BCD code. Additional inputs to U8 allow all outputs to be activated simultaneously (Lamp Test which displays all 8's), all outputs turned off simultaneously (BI/RBO which blanks the display), or the output blanked if the BCD input is zero (RBI). This last input is used in leading zero suppression.

The anode currents of the seven display digits are supplied by the seven individual digit drivers Q1-Q7. These drivers are turned on in sequence by outputs 1 through 7 or U10, and effectively apply the +5 volt adjustable supply to the anodes of the display digits. The segment currents are then determined by the segment drive outputs of U8, and the seven resistors in the output lines. (Active outputs are driven to ground so output currents will be determined by the value of the series resistors.) Corresponding segments of all display digits are wired in parallel, with all seven display digits being driven simultaneously by the 7-line decoder. Only one of these digits is supplied anode current by the digit drivers at any given time. The correct BCD input to U8 is selected by address decoders on the Count Chain (A103).

The zero suppression circuits cause all digits to the left of the first non-zero display to be blanked. Outputs of decoder U10 are processed in U2, U4, U8, and U12, to produce this result.

Decoder outputs of U10 occur in regular time sequence 0 through 7. Defining the interval in which output 0 is active as TF0 (Time Frame 0), then intervals TF0, TF1 . . . . TF7, are of equal length, and occur in a regular repetitive sequence. Display digits are driven in Time Frames TF1-TF7. The zero suppression latches are reset in TF0 of each sequence. The BCD output from A103 is coded to be always zero in TF0. This is decoded in data detector U2 to produce a high at the set input to the U4B latch. U9A output, and U10 TF0 output, are combined in U3 and U7 to produce a reset input to U4B at TF½ (the second half of TF0). U4B is then always reset at the beginning of the TF1-TF7 sequence. During this sequence, the DCU outputs of A103 are addressed and read out in sequence: 10 GHz, 1 GHz . . . 100 kHz. If any of these BCD outputs are non-zero, detector U2 immediately sets U4B. U4B is then reset until the left-most non-zero digit of the display appears after which it remains set through the remainder of each display sequence. This flip-flop is used to remove the suppression when all digits are zero, otherwise the display would disappear completely if there were no input to the counter (zero frequency). The narrow MUX clock is applied to the non-zero data detector via U12 to disable the detector during clock pulses, so switching transients do not cause problems.

Flip-flop U4A controls the zero suppression directly. If U4B is in the set state at the end of a display sequence, then U4A is reset by the clock pulse at TF½ of the next sequence. If U4B is in the reset state at the end of TF7, then U4A is set at TF½ of the next sequence. If non-zero data occurs in a display sequence, U4A is set and enables zero suppression in the next sequence. If all data is zero through a sequence, U4A is set and disables zero suppression in the next sequence. Assuming that many display sequences occur for each set of BCD data, then all zero data receives no suppression, and all zeros are displayed, while non-zero data has leading zeros suppressed.

U4A enables zero suppression in its reset state by applying the low Q output to the ripple blanking RBI input ot U8. With this input low, all decoder outputs are shut off when the data is low and the BI/RBO output is also low. When ever data becomes non-zero, BI/RBO goes high and sets U4A, removing the RBI input enable. This can only be again enabled at the start of a following sequence when U4A may be reset.

GATE INDICATOR DRIVER (U3, U5, U7)

The front panel GATE indicator is driven directly by OR gate U7C in response to the gate trigger from A105. A second input to this gate is obtained from U5 which is also set by the gate trigger via inverter U3E. U5 is a one-shot whose period is set to about 30 ms. The drive pulse to the indicator in response to each gate trigger is then of sufficient duration to be visible, even for very short gate times.

A102 COUNT CHAIN CONTROL

2020084 - G

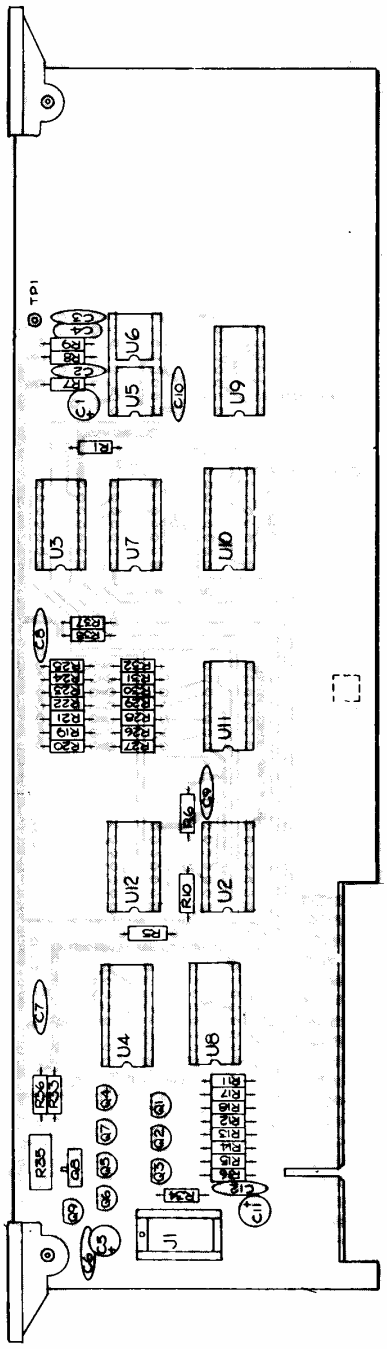
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A102	Count Chain Control	2020084	1	EIP	34257
C1	Tant, 1.0μF, 10%, 35V	2300008	1	TAG20-1/35	14433
C2	Cer.,.001μF, 20%, 1KV	2150001	2	5GA - D10	56289
C3	C2				
C4	Mica, 680pF, 5%, 500V	2250026	1	DM15 - 681V	72136
C5	Tant, 33μF, 20%, 10V	2300015	1	TAG20 - 33/10	14433
C6	Cer., .01μF, 20%, 100V	2150003	6	TG - S10	56289
C7 thru C10	C6				
C11	Tant, 10μF, 20%, 25V	2300029	1	TAG20 - 10/25(M)	14433
C12	C6				
J1	Socket, 14 pin DIP	2630015	1	640357-1	02660
Q1	PNP, RF Amplifier	4710019	7	MPS - D55	04713
Q2 thru Q7	Q1				
Q8	NNPN, Power	4710003	1	MJE - 520	04713
Q9	PPNP, General Purpose	4704126	1	2N4126	04713
R1	Comp, 10, 5%, 1/4 W	4010100	1	RC07GF100J	81349
R2 thru R4	Not Used				
R5	Comp, 2.2K, 5%, 1/4 W	4010222	6	RC07GF222J	81349
R6	R5				
R7	Comp, 22K, 5%, 1/4 W	4010223	1	RC07GF223J	81349
R8	Comp, 10K, 5%, 1/4 W	4010103	1	RC07GF103J	81349
R9	Comp, 100, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R10	R5				
R11	R5				
R12	Comp, 56, 5%, 1/4 W	4010560	7	RC07GF560J	81349
R13 thru R18	R12				
R19	Comp, 1.2K, 5%, 1/4 W	4010122	7	RC07GF122J	81349
R20 thru R25	R19				
R26	Comp, 470, 5%, 1/4 W	4010471	7	RC07GF471J	81349

A102 COUNT CHAIN CONTROL, continued

2020084 - G

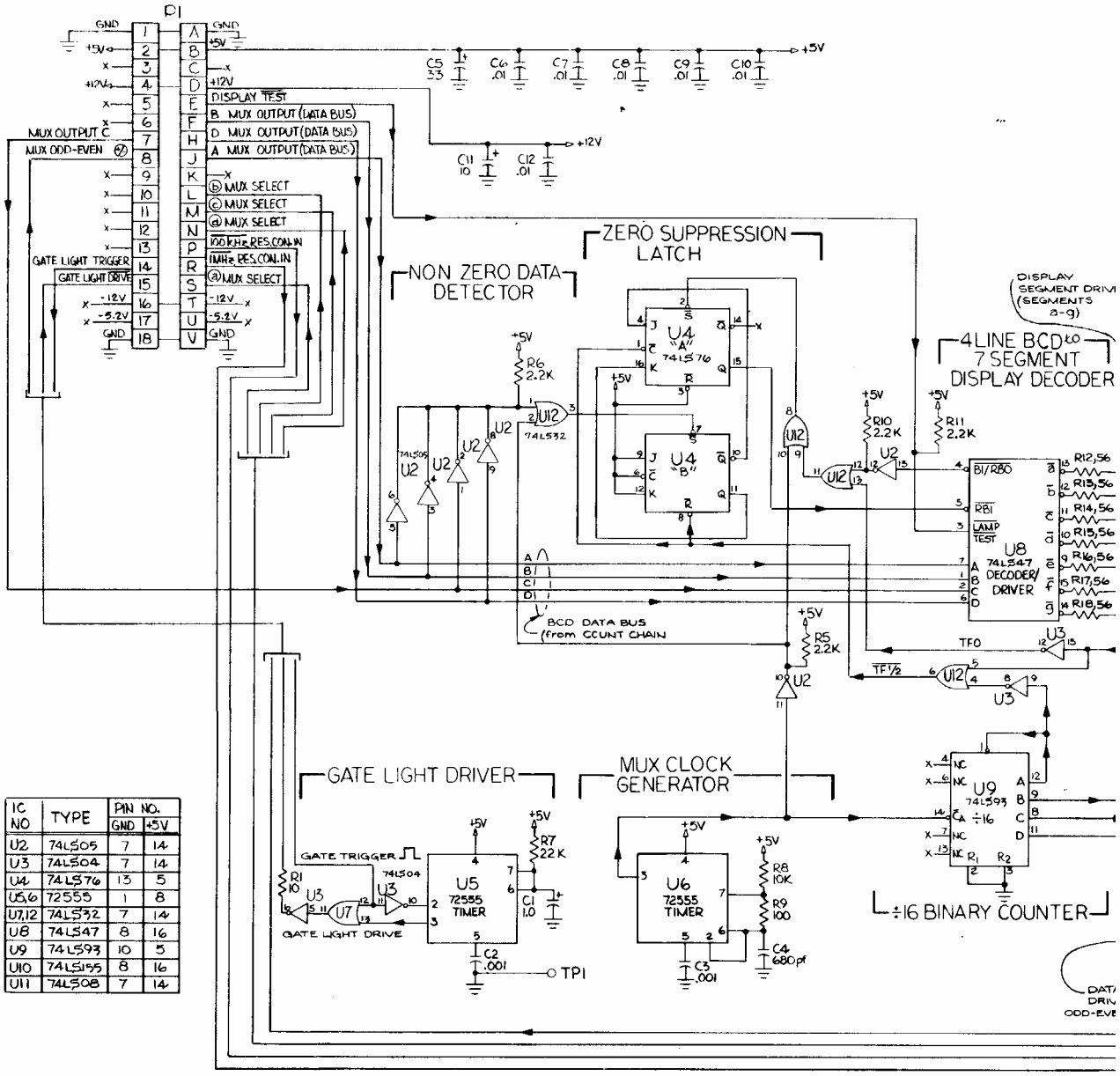
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R27 thru R32	R26				
R33	Comp, 1K, 5%, 1/4W	4010102	1	RC07GF102J	81349
R34	Comp, 820, 5%, 1/4 W	4010821	1	RC07GF821J	81349
R35	Variable, Cer., 500 ohm	4250009	1	72XWR500K	73138
R36	Comp, 180, 5%, 1/4 W	4010181	1	RC07GF181J	81349
R37	R5				
R38	R5				
U1	Not Used				
U2	Hex Inverter	3087405	1	DM74LS05	27014
U3	Hex Inverter	3087404	1	DM74LS04	27014
U4	Dual J-K Preset	3087476	1	DM74LS76	27014
U5	Timer, Linear	3040555	2	NE555V	72136
U6	U5				
U7	Quad, 1 INP, OR Gate	3087432	2	DM74LS32	27014
U8	BCD, 7 seg. Decoder	3087447	1	DM74LS47	27014
U9	4 Bit Binary Counter ÷ 16	3087493	1	DM74LS93	27014
U10	Dual 1-4 Demux, Decoder	3084155	1	DM74LS155	27014
U11	Quad 2INP, AND Gate	3087400	1	DM74LS08	27014
U12	U7				

PAGE LEFT BLANK INTENTIONALLY



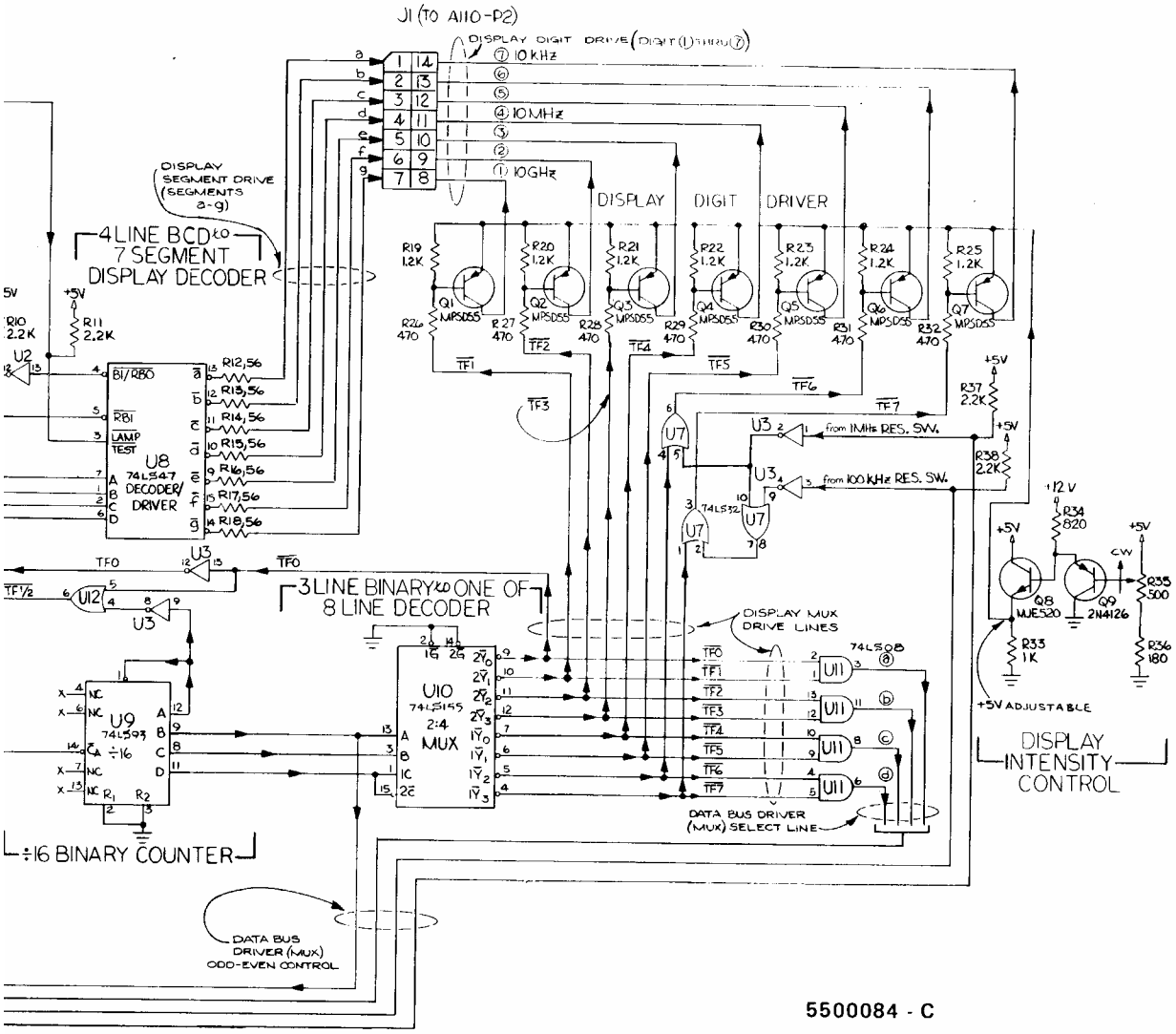
2020084 - G

Figure 102-1. Count Chain Control Component Locator



IC NO	TYPE	PIN NO. GND	+5V
U2	74LS05	7	14
U3	74LS04	7	14
U4	74LS76	13	5
U5,6	72555	1	8
U7,12	74LS32	7	14
U8	74LS47	8	16
U9	74LS93	10	5
U10	74LS155	8	16
U11	74LS08	7	14

LAST REF. DESIG. USED	REF DESIG. NOT USED
R38	R2,3,4
C12	
Q9	
U12	U1
J1	
TP1	



LAST REF. DESIG. USED	REF. DESIG. NOT USED
R38	R2,3,4
C12	
Q9	
U12	U1
J1	
TP1	

Figure 102-2. Count Chain Control Schematic

A103
COUNT CHAIN
(2020083)

The Count Chain board A103 accumulates the counts provided by the output of High Frequency board A106, and on command, stores this BCD information in a separate storage unit. A multiplexer scans the information one digit at a time, and presents the BCD digits serially on a four line output bus. (For Option P4, the same information is presented in parallel form to the rear panel BCD Output connector.) The last three DCU's of the counting chain may be present before normal counting begins.

The 451 Counter measures frequencies by dividing the input frequency in cascaded Decimal Counting Units (DCU's) for a precisely determined gate time. The number of accumulated counts, divided by the gate time, gives the frequency directly. The first DCU is on A106, and is followed by seven additional DCU's on this board. Each DCU has a four-line BCD output to show its accumulated count. These BCD outputs are decoded and drive the front panel display which shows the value of the digits accumulated by each of these DCU's.

COUNTING CHAIN (U16–21)

The counting chain incorporates seven DCU's. The first two are higher speed than the remaining five, as they must operate at higher frequencies. Except for the first DCU, the D output of each DCU directly drives the clock input of the next DCU. The first DCU is presettable by the 1 ms gate command. When this command is not activated, the DCU is held in the "9" state. The DCU carry from the High Frequency board (A106) then bypasses the first DCU and directly clocks the second DCU. When the 1 ms gate command is activated, the preset is removed, and the DCU carry clocks the first DCU which clocks the second. In this state, the first DCU is effectively placed in the count chain. The last three DCU's may be preset to any desired number by applying a load command before normal counting begins. This is used to add the Converter local oscillator frequency to the counting chain to obtain the actual input frequency in Band B.

STORAGE UNIT (U6–12, U14)

Seven 4-bit latches are provided which store the information from the DCU's. The last six are driven directly from the BCD information of each corresponding DCU. The first one is driven from a data selector multiplexer which is controlled by the 1 ms gate command. When this command is not activated, the data selector presents the BCD information from A106 to the latch. When the 1 ms gate command is activated, the data selector selects the BCD information from the first DCU on this board. A load command to all latches, causes the DCU information to be stored and held until the next load command. All information from the counting chain to the balance of the counter, is obtained from these latches.

DATA OUTPUT MULTIPLEXER (U1, U3–5)

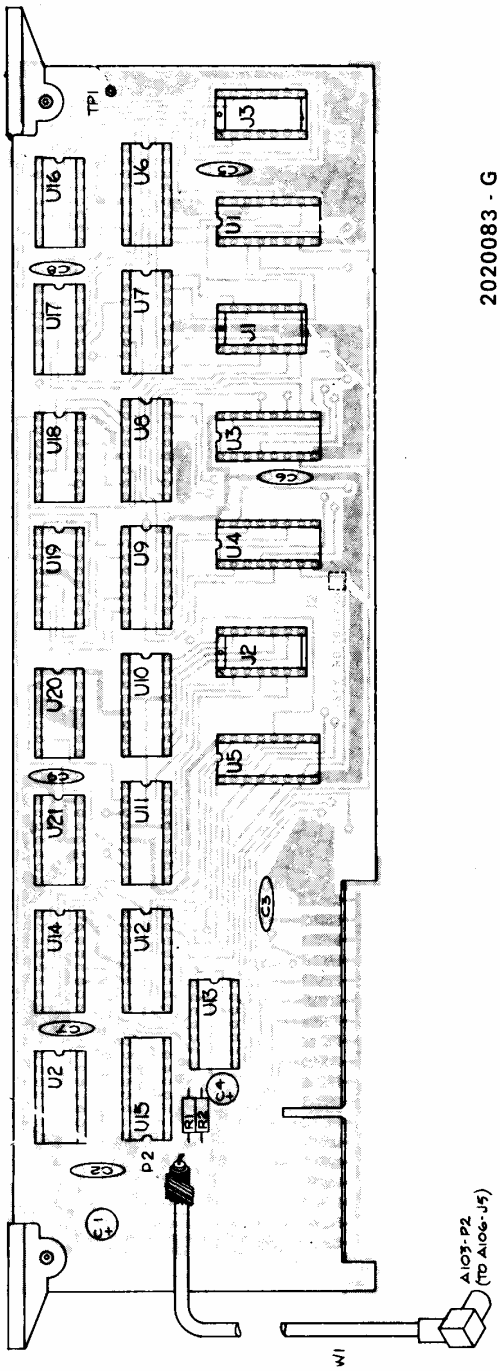
The multiplexer converts the parallel BCD information located in the latches, to the serial form necessary to drive the front panel display. Each multiplexer has tristate outputs – this means that the multiplexer can be gated into an active or passive state. In the passive state, the output is a high impedance which does not respond to the input, thereby allowing the output to be controlled by another IC. Each IC contains four separate channels, with one input and two inputs per channel. A select input to each IC allows one or the other of the inputs to be transferred to the output. The parallel BCD information from the latches is directly applied to the multiplexer inputs. An input select line (MUX Odd/Even), combined with a four-line gating bus (MUX Select Bus), serially selects this BCD information and places it on the multiplexer outputs which are tied together. The end result is serial BCD information which corresponds to the input frequency.

PAGE LEFT BLANK INTENTIONALLY

A103 COUNT CHAIN

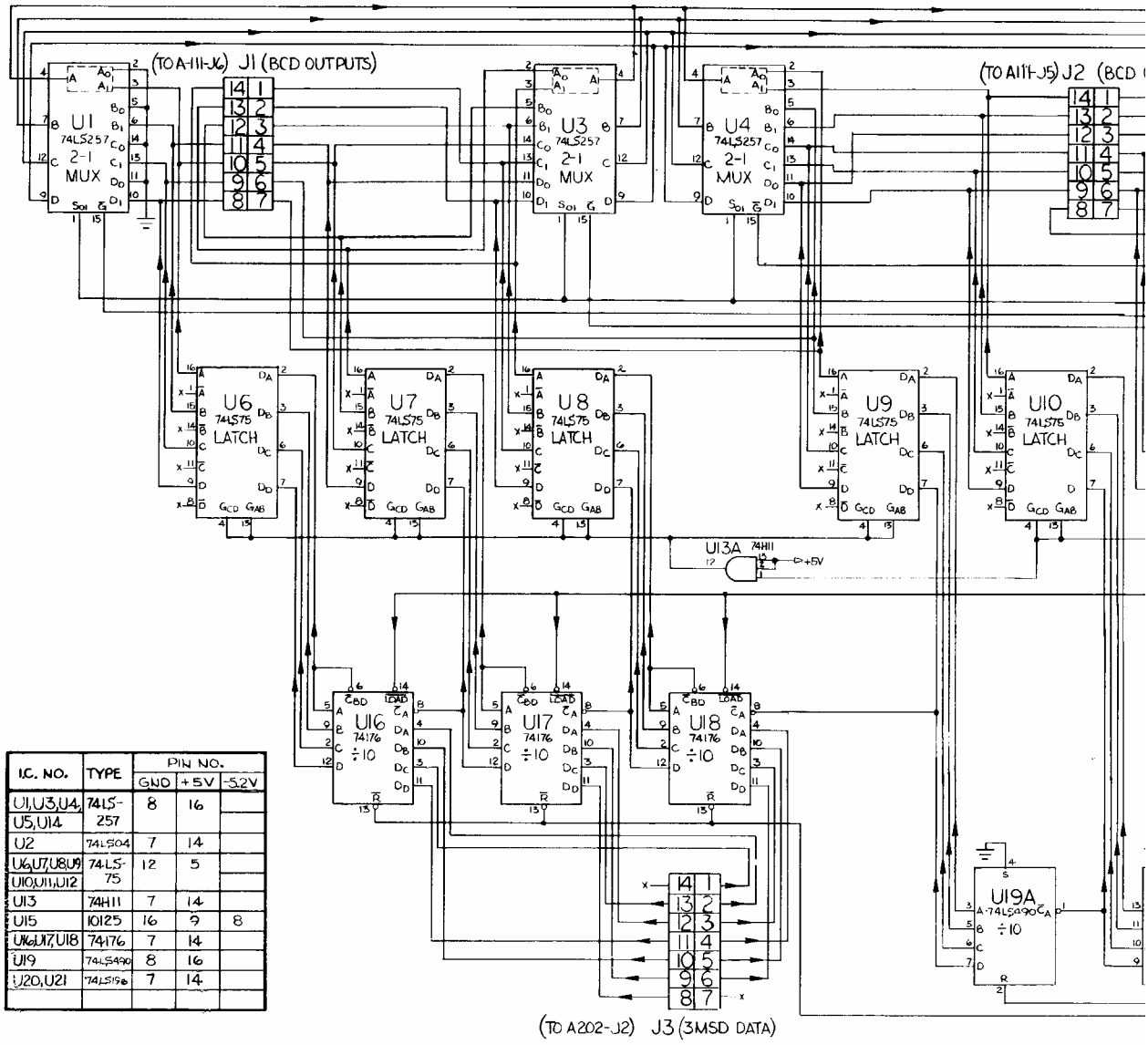
2020083 - G

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A103	Count Chain	2020083	1	EIP	34257
C1	Tant, 33μF, 10%, 10V	2030015	2	TAG 20 - 33/10-50	14433
C2	Cer., .01μF, 20%, 100V	2150003	7	TG S10	56289
C3	C2				
C4	C1				
C5 thru C9	C2				
J1	Socket, 14 Pin	2630015	3	640357-1	02660
J2	J1				
J3 J1					
R1	Met Ox, 180, 2%, 1/4 W	4130181	1	C4/2%/180	24546
R2	Met Ox, 240, 2%, 1/4 W	4130241	1	C4/2%/240	24546
U1	Quad, 2 INP Multiplier	3084257	5	DM74LS257N	27014
U2	Hex Inverter	3087404	1	DM74LS04	27014
U3 thru U5	U1				
U6	Quad Bi-Stable Latch	3087475	7	DM74LS75	27014
U7 thru U12	U6				
U13	3 INP AND Gate	3090004	1	DM74H11P	27014
U14	U1				
U15	Quad Translator	3110125	1	MC10125L	04713
U16	Preset Decade Counter	3074176	3	DM74176N	27014
U17	U16				
U18	U16				
U19	Quad Decade Counter	3084490	1	DM74LS490	27014
U20	PST Decade Counter	3084196	2	DM74LS196	27014
U21	U20				



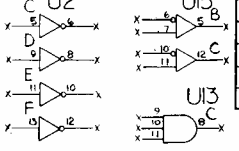
2020083 - G

Figure 103-1. Count Chain Component Locator

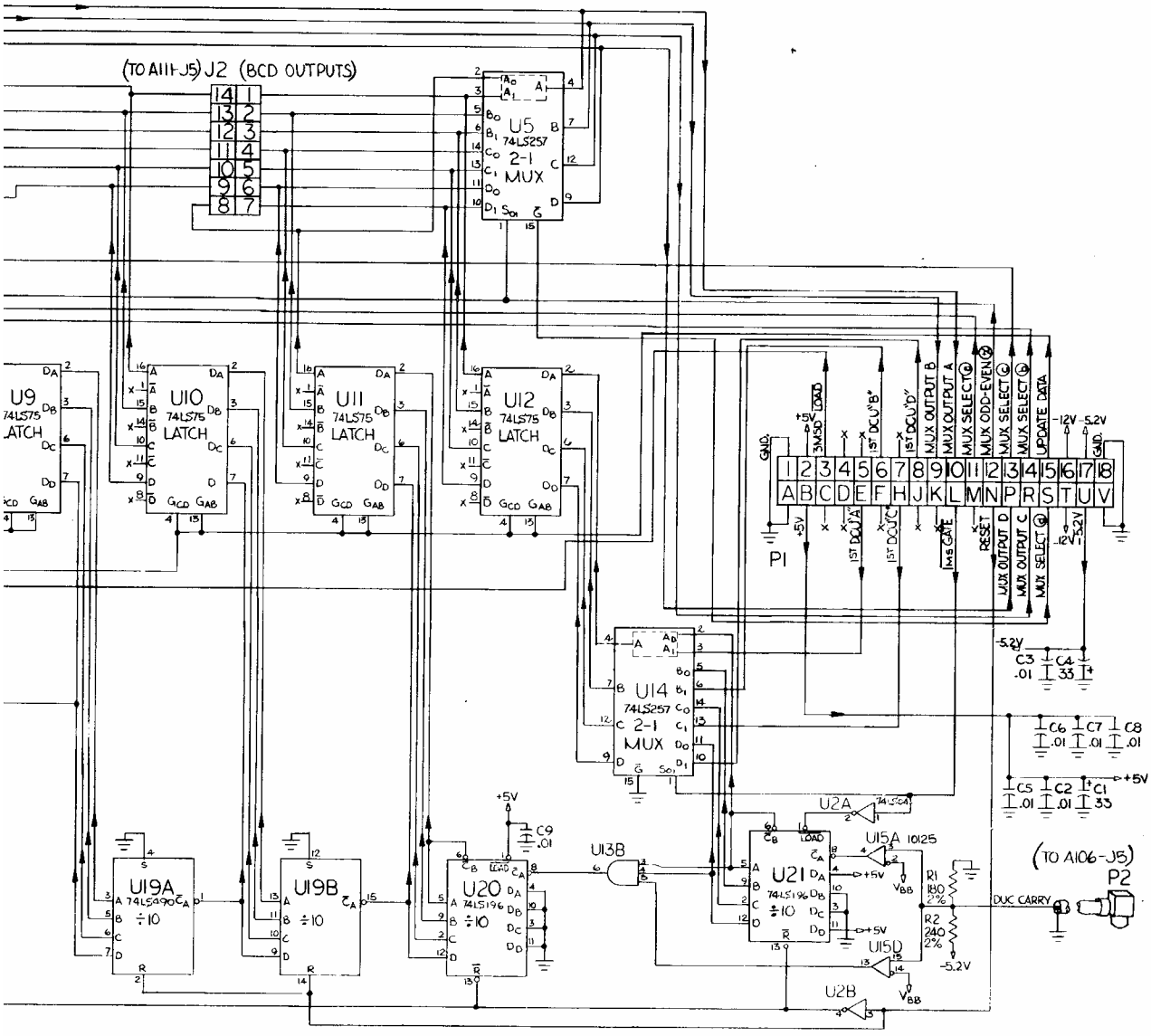


I.C. NO.	TYPE	PIN NO.		
		GND	+5V	-5.2V
U1,U3,U4, U5,U14	74LS-257	8	16	
U2	74LS04	7	14	
U6,U7,U8,U9 U10,U11,U12	74-LS-75	12	5	
U13	74H11	7	14	
U15	10125	16	9	8
U16,U17,U18	74176	7	14	
U19	74LS490	8	16	
U20,U21	74LS195	7	14	

* NOT USED



LAST REF. DESIG. USED	REF. DESIG. NOT USED
R2	
C9	
U21	SEE NOTE *
J3	
P2	



5500083 - B

LAST REF. DESIG. USED	REF. DESIG. NOT USED
R2	
C9	
U21	SEE NOTE *
J3	
P2	

Figure 103-2. Count Chain Schematic

A104
CONTROL INTERFACE
(2020074)

The primary function of this unit is to control and step the counter through the sequence of operations required to measure the freuency of the input signal to the counter.

As with the central processing unit of a computer, generation of this sequence of commands to various portions of the counter is timed by an internal clock. The sequence may be modified by external control inputs, hence the outputs of most panel controls on the counter feed directly to this unit (TEST, BAND, RESET, etc.). Reset always returns the sequence immediately to a fixed starting point.

CONTROL SEQUENCE GENERATOR (U1-5)

This unit produces control signals in sequence on one of sixteen output lines. U5 is a straight scale-of-sixteen binary counter which advances one state each time a clock pulse is applied to its input. The four outputs A, B, C, and D, are applied to two 3-8 line decoders (U3, U4) to produce an output on one of 16 lines corresponding to each of the sixteen possible states of binary counter U5. A reset signal to U5 returns the unit to the start of the sequence with the "0" output line active. A disable input to the decoders allows all outputs to be deactivated at any point in the sequence. This is used during the clock pulse or the reset input to U5 to prevent false outputs on any decoder lines from occurring during times when the counter outputs are in transition between states.

Flip-flop U2A is used to indicate whether the sequence is in one of the states "0" through "9" or in one of the states "10" through "15." After state "9," the frequency measurement is already complete but not yet displayed. The reaction to external interrupts is then different in these two cases.

Flip-flops U1A and U1B are used to produce a much longer than normal step in the control sequence. This allows extra time to read data from the DCU's of the Count Chain in A103 through a multiplexer into latches which hold this data. Output state "11" sets flip-flop U1A which immediately gates off all the decoder outputs via gates U10B, U9B, U11A, and U11B. The sequence generator then operates at full speed in states "12" through a second "12." Flip-flop U1B is set by the D output of U5 while going into state "8," which reactivates the decoder outputs. The output during state "12" is able this time to reset both U1A and U1B, and return the sequence generator to normal operation. The DATA UPDATE output during this long step of the sequence is obtained from U1A rather than from the decoder outputs.

Decoder outputs "13" and "14" are combined in U16 to produce a Print Command pulse twice the duration of the normal sequence outputs.

The control sequence may be frozen in any state by interrupting the clock input to binary counter U5.

CONTROL SEQUENCE

There are 16 output lines from the decoders which are energized in sequence each time the counter repeats a measurement cycle. The operations which correspond to commands on each of these lines 0-15 are listed in Table 104-1.

Any of the normal times listed the table may be extended by interrupting the sequence clock. The times listed as variable in the Table are controlled by internally generated interrupt signals. With Programming Option P4, such an interrupt may be applied from outside the counter. This might occur with a printer, which must freeze the data in the counter until printing is complete. Other interrupts may be generated internally, depending upon the state of the input signal to the counter.

CONTROL SEQUENCE RESET OR INTERRUPT CONDITIONS

The Sequence Generator is rest to its "0" state in a variety of conditions where a measurement has started but cannot be successfully completed. The reset then prevents erroneous data from being displayed or sent out to other remote equipment. The actions that cause these resets include: externally controlled changes of the mode in which the counter operates (band change, Test, etc.), or large changes in the input signal itself before a successful measurement can be completed. The sequence can also be interrupted or reset by direct external commands.

Events which cause both reset of the sequence to "0" and Converter recycle (plus immediate zero display), are as follows:

1. Counter power turn-on.
2. Switch to Band B.
3. End Test in Band B.
4. Reset commands externally or manually applied.

Other events which cause the sequence to be reset to "0":

1. Change of RESOLUTION controls.
2. Switch to Band A.
3. Start Test.
4. End Test in Band A.
5. Start-cycle command from external source.
6. Converter lock or unlock in Band B during sequence "0" - "9."
7. PRF limit signal changes state (input signal appears or drops out) during sequence "0" - "9."

A number of conditions also cause the sequence to be inhibited:

1. A direct Sequence Inhibit command from an external source.
2. Operation of the Display Time Generator. This produces a variable time inhibit controlled by the SAMPLE RATE control or a permanent inhibit with the control at HOLD. A reset (external or manual) command overrides this signal and causes a single sequence before the inhibit is restablished.
3. Operation of the Gate Generator (A105). During Sequence "8" if the counter is in Test or locked to an input signal, the Gate Generator inhibits the sequence until the prescribed gate time is accumulated. Input signal dropout removes this inhibit unless the unit is in the Test mode.
4. PRF limit signal appears (input signal level above threshold) in Band B, but Converter LOCK absent. A delay is produced before sequence continues (or resets) to see if Lock will soon be achieved.
5. LOCK lost in Band B. Time is allowed for relock to a measurable input signal before a reading of zero is produced. This prevents zero readings when lock is broken, even though a measurable input is present continuously.

RESET PULSE TRIGGER GENERATORS

A large proportion of A104 consists of circuits which reset the sequence generator or other portions of the counter. The triggers which operate the reset generators are formed from the various inputs in the same way. The input signals are step functions which are differentiated in RC networks (C16, R37, for example), and coupled through diodes to a common two transistor output stage (Q10, Q11, for example). The TTL compatible output trigger then drives the IC reset generator or gate.

Six inputs to C7-C12 are combined in diodes CR3-CR8 and output stage Q3, Q4 to reset the sequence generator through gate U11D. Four additional inputs to C3-C6 are combined in CR10-CR13 and output stage Q5, Q6 to drive OR gate U22A. During sequence states "0" - "9," this gate drives the first network through CR9 and resets the sequence generator if any input to C3-C6 occurs during states "0" - "9."

SEQUENCE	FUNCTION	DURATION
0	Reset - Resets "0" - "9" Detector.	10 μs
1	Reset - Counting Chain reset to zero.	10 μs
2	Offset Load - Last three DCU's of Count Chain set to any desired number.	10 μs
3	Blank	10 μs
4	Blank	10 μs
5	Blank	10 μs
6	Reset Time Base Generator - Resets Time Base Flip-flop and accumulator on A105.	10 μs
7	Blank	10 μs
8	Signal Gate Enable - Allows Gate Generator (A105) to open the signal gate for the prescribed gate time in response to indication of a measurable input signal to the counter. This is the period when the measurement of input signal frequency actually occurs.	Variable
9	Blank	10 μs
10	Measurement complete - Sets "0" - "9" Detector to show that measurement portion of cycle is complete.	10 μs
11	Update Data - Latches associated with each DCU of the counting chain are latched to new DCU data.	170 μs
12	End Update Data - Resets update data flip-flops.	10 μs
13 14	Print - Sends out signal indicating that new measurement data is available.	20 μs
15	Display - Starts variable time delay, controlled by SAMPLE RATE control, which separates successive measurement cycles.	Variable

TABLE 104-1. CONTROL SEQUENCE

Three inputs to C17-C19 drive a similar network through CR15-CR17, and Q9. These trigger the reset generator one-shot U7A, which produces a uniform pulse about 5 μs in duration. This pulse resets the sequence generator, the display generator, the lock delay generator, and externally the Count Chain and Converter. The Count Chain immediately generates and displays a zero.

The inputs to C18 and C19 are obtained from Schmitt triggers in U9. Inputs to U9 are slow rise signals which are changed to single fast steps by the threshold circuits of U9.

DISPLAY TIME GENERATOR

After each measurement is complete, this unit inhibits the Sequence Generator for a time interval determined by the front panel SAMPLE RATE control. In the HOLD position, the inhibit is permanent until a manual or external reset command is applied, or the power is turned off.

The generator includes a variable period one-shot U7B and DCU U8. The one-shot is connected to produce a free running multivibrator during the delay time. Its output drives the DCU, which extends the period of the one-shot by a factor of ten. The only output of the display generator is a sequence inhibit signal. The DCU outputs are combined to inhibit the sequence, in all but the DCU "9" state. This signal is further combined with the sequence "15" and Fast Cycle controls so that inhibit can occur only in sequence "15" with Fast Cycle not applied and with the display generator DCU not in the "9" state. The Hold input keeps the DCU at "0" state, which applies a permanent sequence inhibit in sequence state "15" as long as Fast Cycle is not applied (or the unit reset).

To start the display time, the DCU is set from the previous "9" state to "0" during Sequence "14." At Sequence "15," the display time one-shot is triggered and commences to free run at a rate determined by the SAMPLE RATE control setting (approximately .3 - 30 pulses per second). Unless held reset by a Hold command, the DCU is stepped at this same rate until it reaches state "9." The sequence inhibit is then removed and the sequence continues normally, thsu ending the display time.

TEST MODE

The circuits involved in test mode generation are primarily Test Flip-flop U2B. The input command is inverted and drives the flip-flop into the set state. It is held in this state until the input command is removed. Sequence Generator "15" output then resets the flip-flop at the end of the measurement cycle. Outputs of the flip-flop reset the sequence generator at start and finish of TEST, supply TEST commands to the Gate Generator (A105) and the High Frequency (A106) boards, remove the Offset Load command in Band B, and remove the Band A and B control signals to A106. The outputs provided the cause the counter to measure an internal 200 MHz test signal as long as the Test Flip-Flop is held set.

PRF LIMIT

The PRF Limit circuits receive the input threshold signal from Gate Generator A105. This signal is present whenever the input signal to the counter is above the preset threshold level, and absent when it is below this level. The PRF circuit then produces a continuous output unless gaps in the input exceed about 100 ms, indicating a dropout of the input signal. The PRF Limit Disable input, when active, causes the PRF circuit to produce a permanent high output, despite the disappearance of the input signal.

The PRF circuit includes a one-shot (U6A), triggered by the step which occurs when the input threshold signal disappears. The threshold signal also produces a fast-fall, slow-rising output from inverter U4A with C14, R25, and R26 load. This signal and the one-shot Q output are combined in NAND gate U20D to produce a signal that rises rapidly with appearance of the threshold signal. It does not fall however, unless the threshold signal stays low for more than 100 ms (the time constant of the one-shot).

A104 CONTROL INTERFACE

2020074 -M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A104	Control Interface	2020074	1	EIP	34257
C1	Cer., .01μF, 20%, 100V	2150003	6	TG - S10	72982
C2	Tant, 100μF, 20%, 6.3V	2300024	1	TAG 20-47/6.3-50	14433
C3	Cer., .001μF, 20%, 1KV	2150001	13	SGA - D10	56289
C4	C3				
C5	Mica, 200pF, 5%, 500V	2250009	1	DM - 15 - 200J	72136
C6 thru C12	C3				
C13	Tant, 33μF, 20%, 10V	2300015	4	TAG 20-33/10	14433
C14	C1				
C15	Tant, 10μF, 20%, 25V	2300029	2	TAG 20-10/25	14433
C16	C15				
C17 thru C20	C3				
C21	C13				
C22	C1				
C23	C1				
C24	C1				
C25	C13				
C26	C1				
C27	C13				
CR1 thru CR18	General Purpose	2704154	18	IN4154	07263
Q1	NPN General Purpose	4704124	8	2N4124	04713
Q2	PNP General Purpose	4704126	5	2N4126	04713
Q3	Q1				
Q4	Q2				
Q5	Q2				
Q6 thru Q9	Q1				
Q10	Q2				
Q11	Q1				
Q12	Q1				
Q13	Q2				
R1	Comp, 2.2K, 5%, 1/4 W	4010222	11	RC07GF222J	81349
R2	Comp, 3.3K, 5%, 1/4 W	4010332	2	RC07GF332J	81349
R3	Comp, 10, 5%, 1/4 W	4010100	4	RC07GF100J	81349
R4	R3				

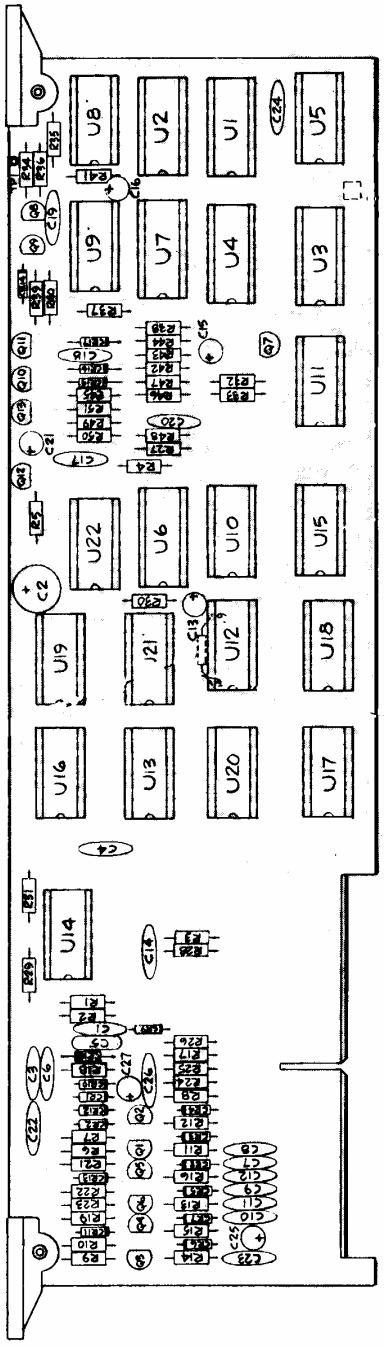
A104 CONTROL INTERFACE, continued 2020074-M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R5	Comp, 47K, 5%, 1/4 W	4010473	1	RC07GF473J	81349
R6	R1				
R7	Comp, 5.6K, 5%, 1/4 W	4010562	5	RC07GF562J	81349
R8	Comp, 10K, 5%, 1/4 W	4010103	7	RC07GF103J	81349
R9	R1				
R10	R7				
R11	Comp, 1K, 5%, 1/4 W	4010102	15	RC07GF102J	81349
R12					
thru					
R16	R11				
R17	R8				
R18	R11				
R19	R11				
R20	Not Used				
R21	R11				
R22	R7				
R23	R1				
R24	R8				
R25	R1				
R26	R2				
R27	Comp, 18K, 5%, 1/4 W	4010183	1	RC07GF183J	81349
R28	R3				
R29	R1				
R30	R3				
R31	R1				
R32	Comp, 820, 5%, 1/4 W	4010821	1	RC07GF821J	81349
R33	R8				
R34	R11				
R35	R1				
R36	R1				
R37	Comp, 100, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R38	Comp, 3.9K, 5%, 1/4 W	4010392	1	RC07GF392J	81349
R39	R11				
R40	R11				
R41	R1				
R42	R11				
R43	R11				
R44	R11				
R45	R8				
R46	R7				
R47	R1				
R48	R8				
R49	R7				
R50	Comp, 2.7K, 5%, 1/4 W	4010272	1	RC07GF272J	81349
R51	Comp, 39K, 5%, 1/4 W	4010393	1	RC07GF393J	81349
R52	R8				

A104 CONTROL INTERFACE, continued

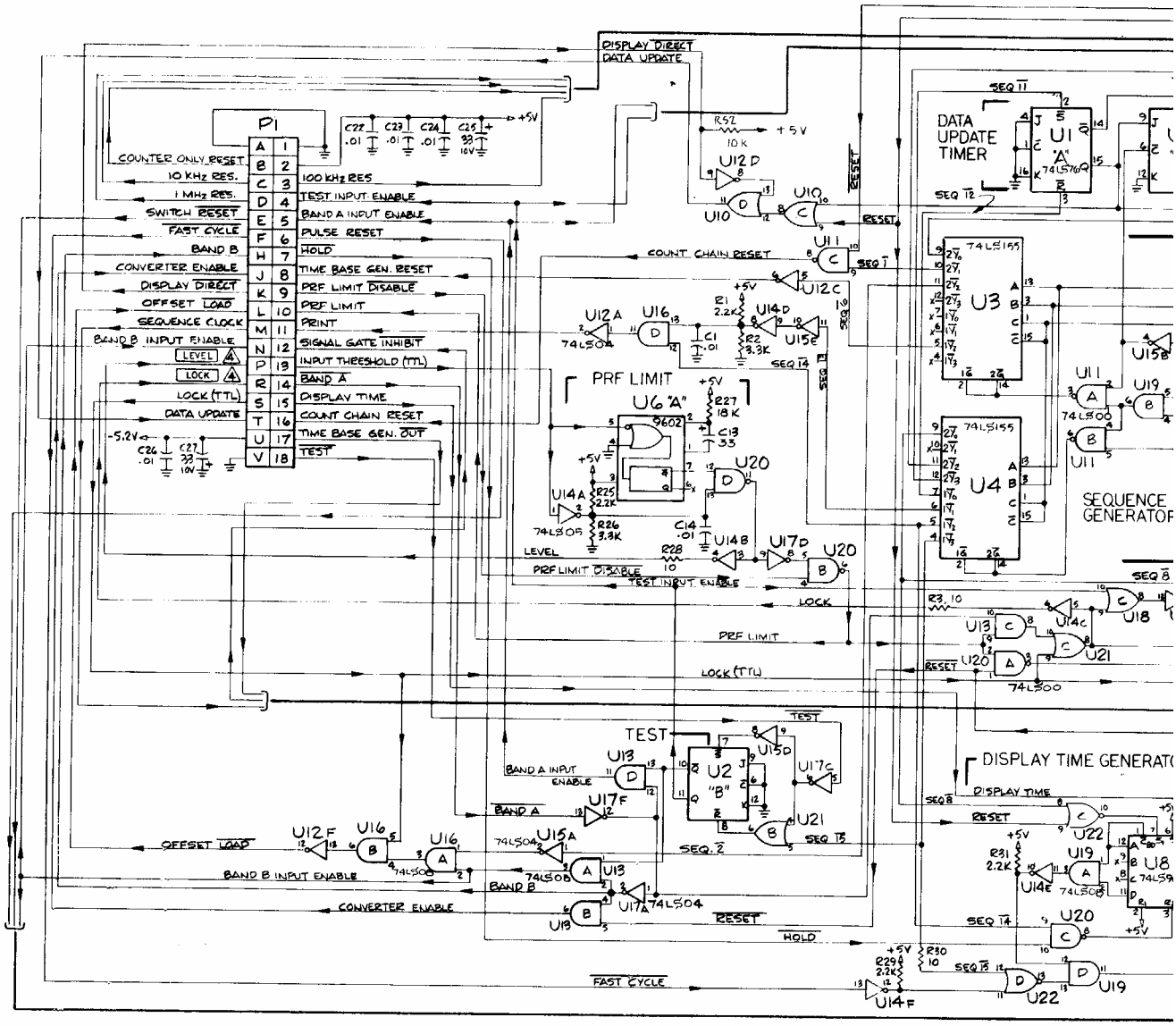
2020074 -M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U1	Dual J-K Preset	3087476	2	DM74LS76	27014
U2	U1				
U3	Dual 1-4 Demux	3084155	2	DM74LS155	27014
U4	U3				
U5	4 Bit Bianary Counter	3087493	1	DM74LS93	27014
U6	Digital Dual, Mono Stable, MV	3009602	2	DM9602N	27014
U7	U6				
U8	Decade Counter	3087490	1	DM74LS90	27014
U9	Dual 4 INP SHMT Trigger	3087413	1	DM74LS13	27014
U10	Quad 2 INP OR Gate	3087432	3	DM74LS32	27014
U11	Quad 2 INP NAND Gate	3087400	2	DM74LS00	27014
U12	Hex Inverter	3087404	3	DM74LS04	27014
U13	Quad 2 INP AND Gate	3087408	3	DM74LS08	27014
U14	Hex Inverter	3087405	1	DM74LS05	27014
U15	U12				
U16	U13				
U17	U12				
U18	U10				
U19	U13				
U20	U11				
U21	U10				
U22	Quad 2 INP NOR Gate	3087402	1	DM74LS02	27014



2020074 - M

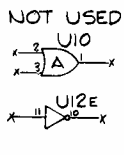
Figure 104-2. Control Interface Component Locator



I.C. NO	TYPE	PIN NO GND	PIN NO +5V	NOT USED
U1, U2	74LS76	13	5	
U3, U4	74LS155	8	16	
U5	74LS93	10	5	
U6, U7	9602	8	16	
U8	74LS90	10	5	
U9	74LS13	7	14	9,11
U10, U18, U21	74LS32	7	14	
U11, U20	74LS00	7	14	
U12, U15, U17	74LS04	7	14	
U13, U16, U19	74LS08	7	14	
U14	74LS05	7	14	
U22	74LS02	7	14	

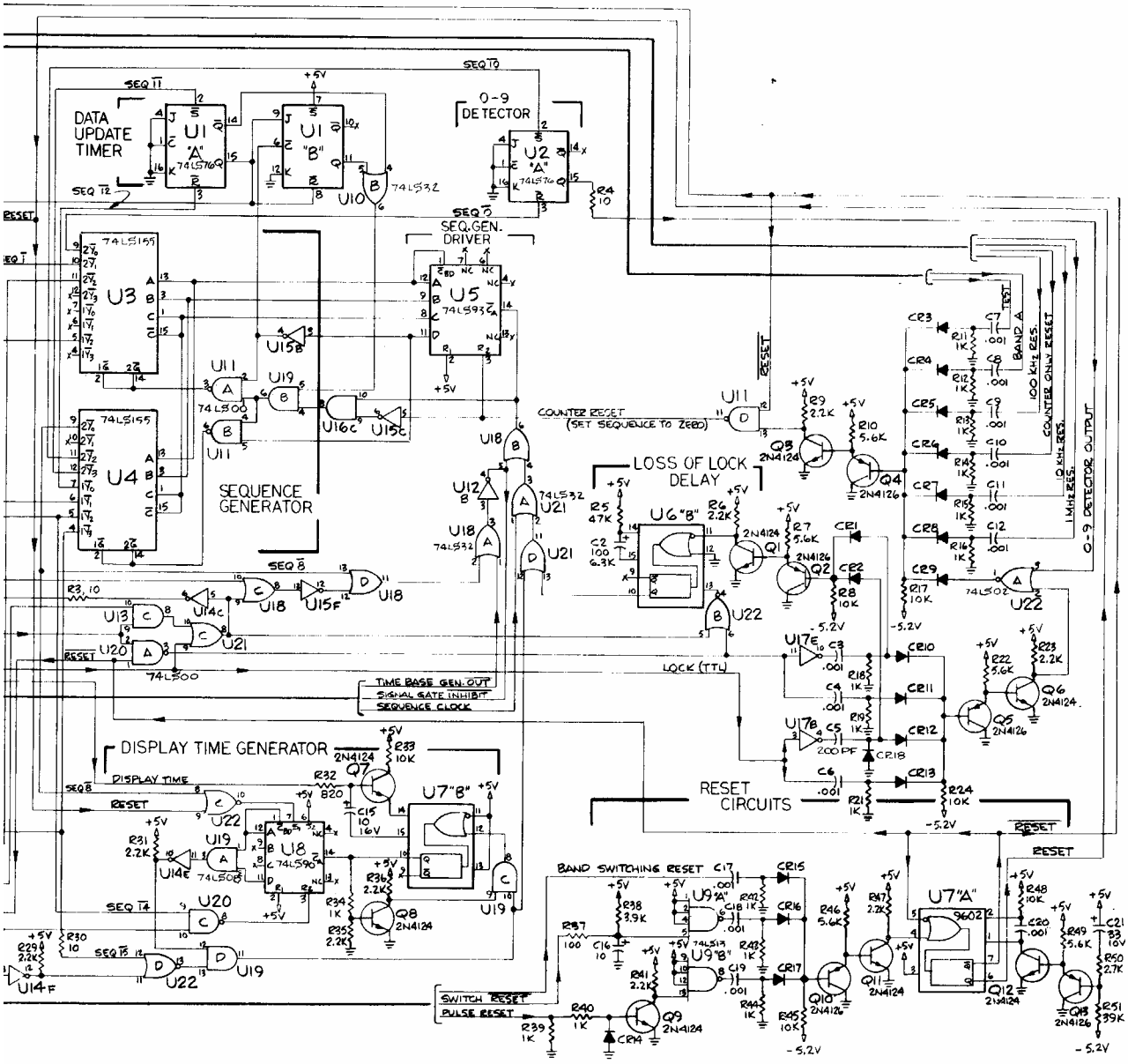
LAST REF DESIG USED	NOT USED
C27	
CR17	
Q13	
R52	
U22	

NOT USED



⚠ BOX [ ] DENOTES FRONT PANEL INDICATOR.

8. ALL DIODES ARE 1N4154.



5500074 - F

Figure 104-3. Control Interface Schematic

A105
GATE GENERATOR
(2020085)

This unit produces the gate signal which controls the time intervals over which the input to the counter is accumulated. It also produces the 100 kHz Control Sequence Clock, and a 200 MHz Test signal. These outputs are all based on 200 MHz and 10 MHz references supplied from other portions of the counter.

GATE AND ENABLE FLIP-FLOPS (U2A/B)

The flip-flops are dual ECL types, both clocked by the same 200 MHz reference signal. The Gate Flip-flop controls the main counter signal gate directly, while the Enable Flip-flop determines which cycle of the 200 MHz clock will trigger the Gate Flip-flop.

The enable signal to the Enable Flip-flop, is derived from the counter input threshold circuit, and is present only at times when an input signal of adequate amplitude is present. This signal is combined with a signal from Control board A104, which indicates that the counter is in the correct part of its cycle to actually measure the input signal frequency. The rise time of the enable signal is faster than the clock period, so the Enable Flip-flop will always settle definitely into one of its two stable states when any individual clock pulse arrives.

The output of the Enable Flip-flop is applied to the enable input of the Gate Flip-flop which is triggered to the corresponding state by the next 200 MHz clock pulse. Transistions of the Gate Flip-flop occur only at a defined trigger point on the clock pulse, which is timed very accurately ($<<1$ ns from periodic 200 MHz). The output of the Enable Flip-flop is also combined with the output of the Time Base Flip-flop (U2B). This allows only a specified number of clock pulses to occur during the gate time of each measurement cycle of the counter. Accumulated gate times are: 1 ms or 100 μs (4 ms or 400 μs in Band A). The Gate control signal is applied via a 50 ohm cable to the signal gate on A106.

TIME BASE FLIP-FLOP (U3B)

This is another fast ECL flip-flop. It is clocked by a 200 MHz signal, slightly delayed from that driving the Enable and Gate Flip-flops. The delay allows the Gate Flip-flop (triggered by the normal clock), to control the delayed clock during the same clock period in which the Gate Flip-flop changes state. The clock delay and propagation delay through the flip-flop, are approximately equal. The Time Base Flip-flop is reset at the beginning of each measurement cycle, removing the disable signal applied by it, to the Gate Flip-flop.

During the gate enable portion of the counter control sequence, the Gate Flip-flop is controlled by the input threshold circuits via the Enable Flip-flop and the 200 MHz clock. Each time the Gate Flip-flop opens the Signal Gate, the 200 MHz delayed clock is also applied to the Time Base Accumulator and to the Time Base Flip-flop clock input. The clock pulse which opens the signal gate is ignored. All pulses which occur during a Signal Gate open period are recognized, including the one which closes the Gate. Coincidence circuits in the Time Base Accumulator produce signals when N-4 and N-3 clock pulses have been applied to the Accumulator. N is the number of clock periods required to produce the desired accumulated gate time. The N-4 signal is applied to the clock enable input, and the N-3 signal to the enable input of the Time Base Flip-flop. The N-2 clock pulse then actually triggers the Time Base Flip-flop to its set state. The delay already present in the delayed clock driving the accumulator, is extended by a delay network following the Time Base Flip-flop. The disable signal from the Time Base Flip-flop to the Gate Flip-flop input is then delayed until after the N-1 normal clock pulse. The N clock pulse resets the Gate Flip-flop, and ends gate time for that measurement cycle.

TIME BASE ACCUMULATOR (U3A, U5, U10-12)

The Time Base Accumulator includes five DCU's (U5, U11, U12), preceded by a binary divider. The count capacity of this group is 200K clock pulses, each of 5 ns period, or 1 ms total. The last DCU may be removed from the string to permit a 100 μs gate time. In addition to the string of DCU's, a ÷4 unit is included between the first and second DCU's, which may be switched into or out of the chain. The ÷4 is included when operating in Band A, to increase the gate time by a factor of four. The input to A106 is divided by four before reaching the Signal Gate, so the gate time must be extended to cause the counter to read the input frequency directly.

A coincidence detector consisting of U7A, U8, U9, U14D, Q4, CR1, and the D output of U5, produces an output when all DCU's of the string are in state "9," and the ÷4 unit is in state "3." The first DCU of the string is preset to 9 originally, giving coincidence after N-2, rather than N-1 clock pulses to the first DCU. (Driving C_{BD} input with the A, rather than the inverted A output, is equivalent to a preset 9.) Since the accumulator clock input is divided by two in binary U10A before the first DCU, coincidence output occurs in the N-4 input pulse.

Since coincidence occurs when all DCU's are at 9, and the ÷4 at 3, any one of them is effectively removed from the string if held at these counts. U12B has an external set 9 input to produce the shorter 100 μs gate time in this manner. This ÷4 unit may also be held at 3 by an external control signal (Band B or Test), but additional gating must be provided to pass the input signal around the stage, since the following DCU's still have to operate. This is accomplished in U8B, which transmits either the input or output of U10 to the input of U11A.

The ÷2, and the first DCU of the Accumulator, are fast ECL circuits, able to divide the 200 MHz clock to 10 MHz; the remaining circuits are TTL.

BAND SELECT CIRCUITS (U4B-D, U7B/C, U14A)

These circuits select one of the Band Threshold signals from either the Converter (Band B) or Prescaler (Band A), and processes this to control the Enable and Gate Flip-flops. U7C is simply a buffer/inverter which is driven by a level derived from the front panel BAND SELECT switch. The buffer output drives one input of U4B, while the inverter output drives one input of U4C, such that one of the pair U4B/U4C is always enabled, and one disabled. The inverting outputs of U4B and U4C are "ORed" together to drive one U4D input. The direct out-of U4B is now a replica of the envelope of the signal to the selected input to the counter – being high if the signal is above threshold level, and low if the signal is less than threshold. The second input to U4D is high in the Test mode, so the Gate Flip-flop operates as if the 200 MHz Test signal is always above threshold level.

The output of U4D to the Enable Flip-flop goes low whenever the input signal to the counter is above threshold. A capacitor to ground slows the fall of this transistion without great effect on the risetime. The signal is squared up again in U1C to produce an Enable signal which is delayed from the rise of the input signal to threshold, but disappears without delay as the input drops below threshold. This delays counting of the input signal until irregularities on the rise of the RF pulse have died out.

CONTROL SEQUENCE CLOCK GENERATOR (U14-16)

This circuit divides the input 10 MHz reference by 100 to form the 100 kHz Sequence Clock. The input accepts a wide variety of input levels and waveshapes, while producing a square wave of the proper level to drive U16. U15B gates the outputs of U16 to form 100 ns pulses at a 100 kHz rate. U14C allows the Clock to be gated by an external control level.

A105 GATE GENERATOR

- 2020085 - J

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A105	Gate Generator	2020085	1	EIP	34527
C1	Cer., .01μF, 20%, 100V	2150003	17	TG - S10	56289
C2	Not Used				
C3	Not Used				
C4	C1				
C5	Mica, 39pF Nom - S.A.T.	2250999	1		
C6	C1				
C7	Mica, 120pF Nom S.A.T.	2250999	1	DM15 - 121J	72136
C8 thru C13	C1				
C14	Tant, 33μF, %, 10V	2300015	2	TAPA 33M10	14433
C15	C1				
C16	C1				
C17	Tant, 10μF, %, 25V	2300029	1	DF106M25S	72136
C18 thru C22	C1				
C23	C14				
C24	C1				
CR1	General Purpose	2704154	1	IN4154	07263
J1 thru J4	Jack, PC Rcpt Str	2610018	4	51-051-0000	98291
Q1 thru Q3	Not Used				
Q4	RF Graded, PNP, YEL	4710012	1	4705179	EIP
R1 thru R4	Not Used				
R5	Comp, 68, 5%, 1/4 W	4010680	1	RC07GF680J	81349
R6	Comp, 200, 5%, 1/4 W	4010201	1	RC07GF201J	81349
R7 thru R11	Not Used				
R12	Comp, 300, 5%, 1/4 W	4010331	8	RC07GF331J	81349
R13	R12				
R14	R12				
R15	Comp, 1K, 5%, 1/4 W	4010102	2	RC07GF102J	81349
R16	Comp, 390, 5%, 1/4 W	4010391	5	RC07GF391J	81349

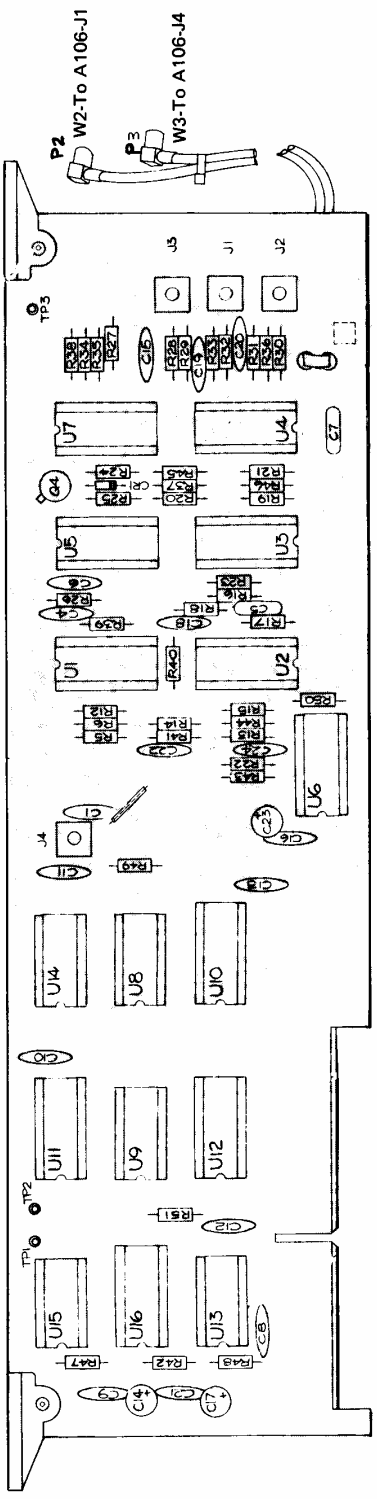
A105 GATE GENERATOR , continued 2020085 - J

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R17	Comp, 18, 5%, 1/4 W	4010180	1	RC07GF180J	81349
R18 thru R20	R12				
R21	Comp, 470, 5%, 1/4 W	4010471	6	RC07GF471J	81349
R22	R21				
R23	R16				
R24	Met Ox, 1.8K, 2%, 1/8W	4130182	3	C4/2%/1.8K	24546
R25	Met Ox, 390, 2%, 1/8 W	4130391	1	C4/2%/390	24546
R26	Comp, 27, 5%, 1/4 W	4010270	1	RC07GF270J	81349
R27	R16				
R28	Comp, 150, 5%, 1/4 W	4010151	1	RC07GF151J	81349
R29	R12				
R30	Met Ox, 82, 2%, 1/4 W	4130820	2	C4/2%/82	24546
R32	R30				
R33	R31				
R34	R21				
R35	R31				
R36	R12				
R37	Comp, 2.2K, 5%, 1/4 W	4010222	3	RC07GF222J	81349
R38	R16				
R39	Comp, 100, 5%, 1/4 W	4010101	2	RC07GF101J	81349
R40	R15				
R41	R21				
R42	Met Ox, 1.2K, 2%, 1/4 W	4130122	1	C4/2%/1.2K	24546
R43	R24				
R44	R24				
R45	R21				
R46	R16				
R47	Met Ox, 3.6K, 2%, 1/4 W	4130362	1	C4/2%/3.6K	24546
R48	Met Ox, 1.5K, 2%, 1/4 W	4130152	1	C4/2%/1.5K	24546
R49	R37				
R50	R39				
R51	R37				
U1	Triple Line Receiver	3110216	1	04731	
U2	Dual High Speed Flip-Flop	3110231	2	04731	
U3	U2				
U4	NOR Gate	3110102	1	04731	
U5	Counter	3110138	1	04731	
U6	Quad Translator	3110125	1	04731	
U7	Quad Translator	3110124	1	04731	
U8	Dual 4 INP AND Gate	3090003	2	27014	
U9	U8				
U10	Dual J-R Flip-Flop	3087476	1	27014	

A105 GATE GENERATOR , continued

2020085 - J

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U11	Dual Decade Counter	3084490	3	DM74LS490	27014
U12	U11				
U13	Hex Inverter	3087404	1	DM74LS04	27014
U14	Quad 1 INP NOR Gate 3087402	3087402	1	DM74LS02	27014
U15	Dual 4 INP NAND Trigger	3087413	1	DM74LS13	27014
U16	U11				



2020085 - J

Figure 105-1. Gate Generator Component Locator

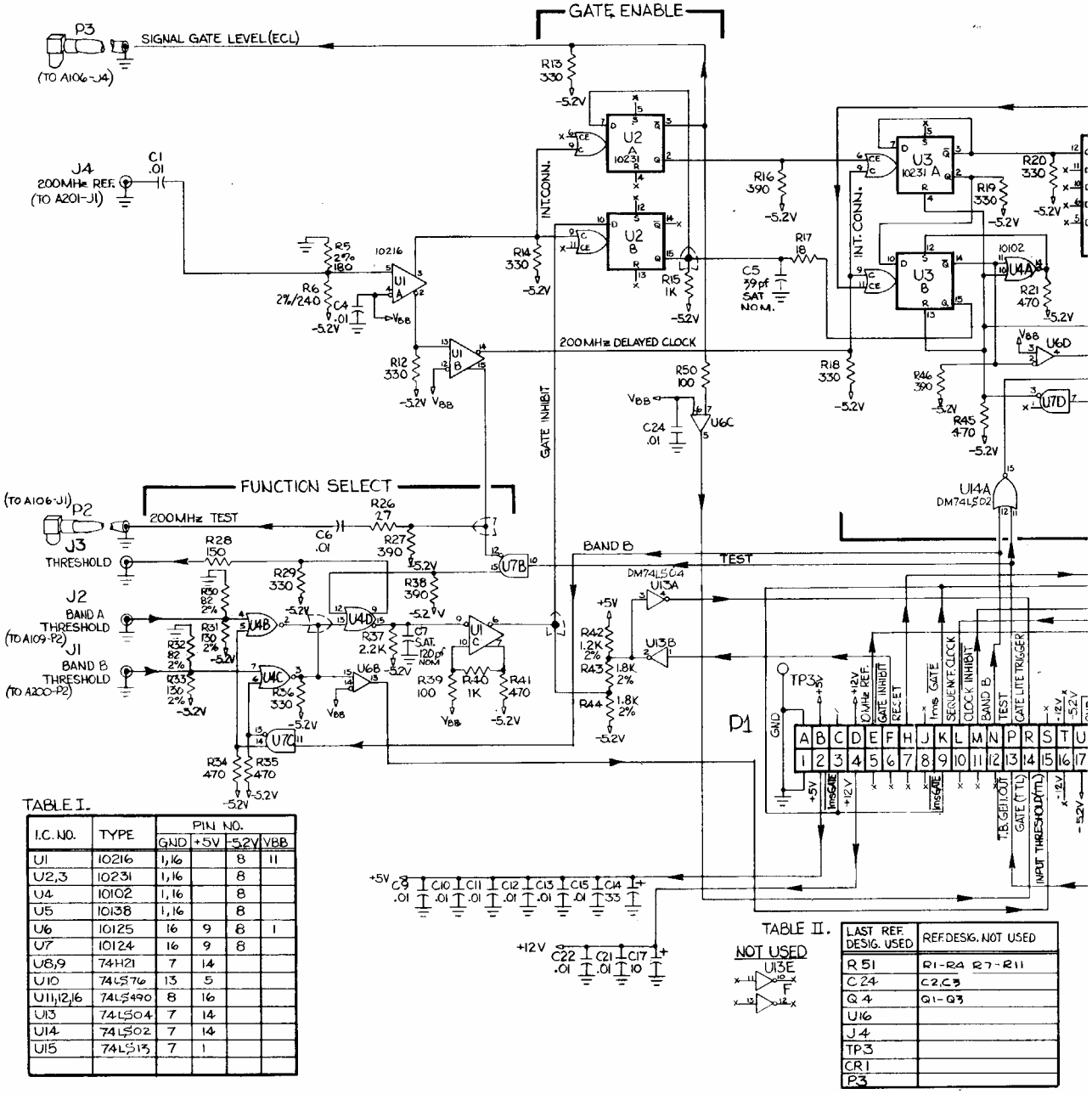
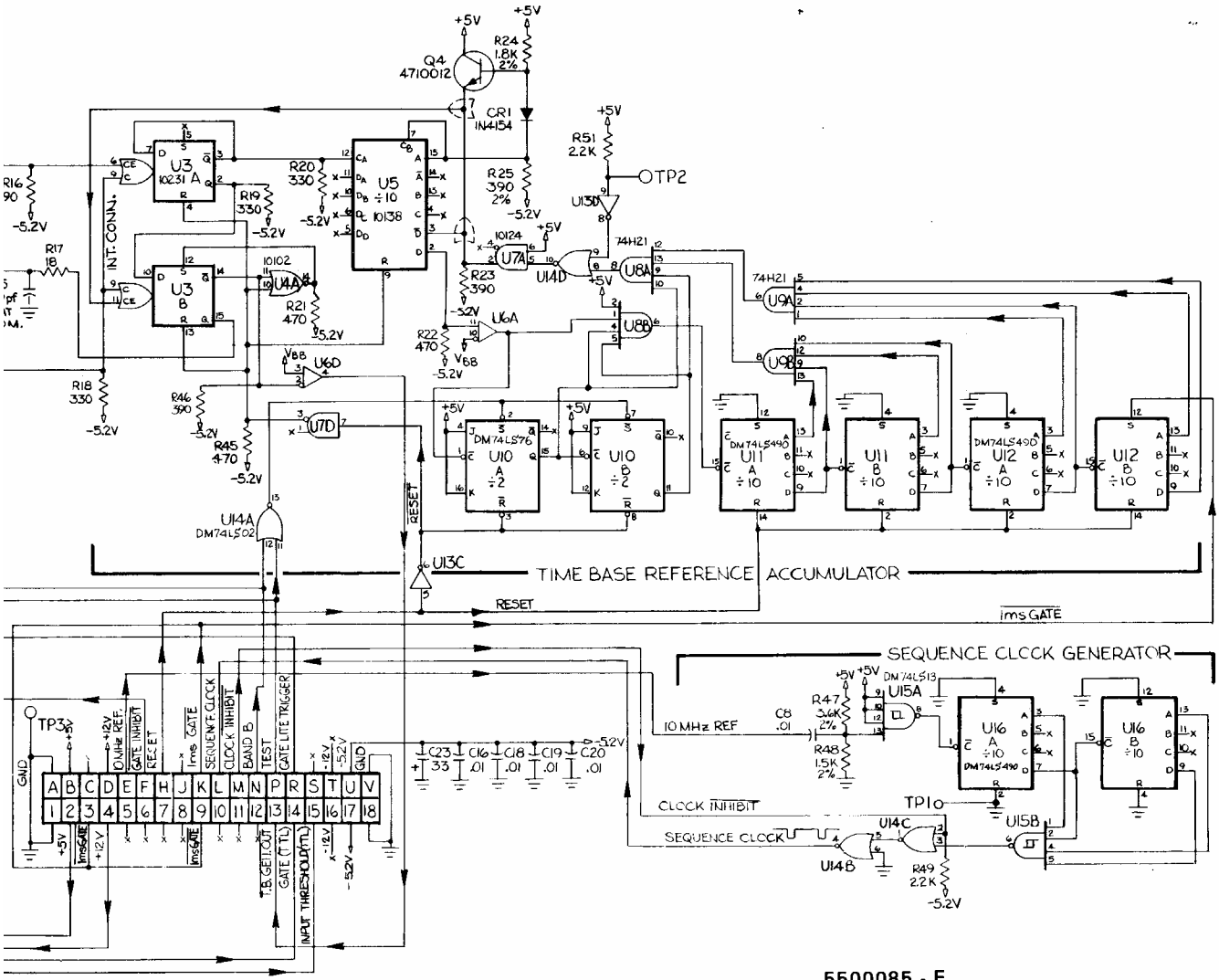


TABLE I.

I.C. NO.	TYPE	PIN NO.			
		GND	+5V	-5.2V	VBB
U1	10216	1,16		8	11
U2,3	10231	1,16		8	
U4	10102	1,16		8	
U5	10138	1,16		8	
U6	10125	16	9	8	1
U7	10124	16	9	8	
U8,9	74H21	7	14		
U10	74LS76	13	5		
U11,12,16	74LS490	8	16		
U13	74LS04	7	14		
U14	74LS02	7	14		
U15	74LS13	7	1		

TABLE II.

LAST REF. DESIG. USED	REF. DESIG. NOT USED
R51	R1-R4 R7-R11
C24	C2,C3
Q4	Q1-Q3
U16	
J4	
TP3	
CR1	
P3	



5500085 - E

TABLE II.

LAST REF. DESIG. USED	REF. DESIG. NOT USED
R 51	R1-R4 R7-R11
C 24	C2,C3
Q 4	Q1-Q3
U16	
J 4	
TP3	
CR1	
P3	

I USED
U13E
F

Figure 105-2. Gate Generator Schematic

A106
HIGH FREQUENCY
(2020081)

The High Frequency board provides the initial signal processing and first decade of counting for the Direct Counter. It selects and processes one of three input signals: the Converter IF output, the Prescaler divide-by-four output, and the 200 MHz Test signal. BCD information and the divide-by-ten output from the first decade counting unit are sent from this board to the Count Chain board (A103) for further counting and display.

One of the three input signals is selected by enabling one of three differential amplifiers: U1B, U2A, or U2B. U1A provides additional gain for the Converter IF signal when input U1B is selected. Enabling of the appropriate amplifier is achieved by activating transistor Q2, Q3 or Q4, by TTL Band Select commands entering on P1.

The output of the input selector differentially drives the squaring circuit. Q5 is a current mirror, which is used as an overdriven voltage-to-current converter. The collector current of Q5 drives the pulse forming network which begins with a wide-band, high-speed differential amplifier (Q6/Q7). The output of this differential amplifier drives Q8, which is used as a current switch. The resulting current square wave from Q8 drives inductor L4, producing a series of pulses – a positive pulse when Q8 turns on, and a negative pulse when Q8 turns off.

The pulse inverter is essentially a high-speed zero bias amplifier. Q9 performs this function by being biased at cut-off by diode CR4. In this mode, the amplifier not only inverts the positive pulses, but removes the unwanted negative pulses. The output of the pulse inverter drives the input of decade divider U4. The bias point for U4's input is established by a tracking bias supply (U3/Q10). The output of U3 is equal to the voltage on U4 pin 1, plus a fixed DC offset selected by resistor divider R47/R49. The divide-by-ten output of the decade divider is a 60/40 duty cycle ECL level signal called "DCU CARRY." The load resistor for this signal is located on the Count Chain board (A103) to provide a termination for the connecting co-ax cable.

The BCD output information is available on P1 pins 11-14. During a count cycle at high frequencies, this information is slew rate limited, therefore the actual output levels cannot be seen until the circuit comes to rest. After the circuit is finished counting, TTL level signals are present on these outputs. The decade divider is reset after the counting cycle is complete by a TTL reset signal on U4 pin 3. This signal comes into the board via P1 pin 10.

The gate signal (an inverted ECL level logic signal) enters the board at J4, and passes through U6. The first stage is an input buffer whose threshold signal (U6 pin 5) is derived from op amp temperature-compensated bias supply U5. U5's function is similar to U3 with the output tracking the reference voltage (U6 pin 11), plus some fixed offset supplied by voltage divider R59-R61. This accommodates slight changes in threshold which produce the effect of a change in gate width.

The gate output to the rear panel is supplied by the Gate Output Buffer, consisting of Q11, Q12, and associated circuitry.

PAGE LEFT BLANK INTENTIONALLY

A106 HIGH FREQUENCY

2020081 - M

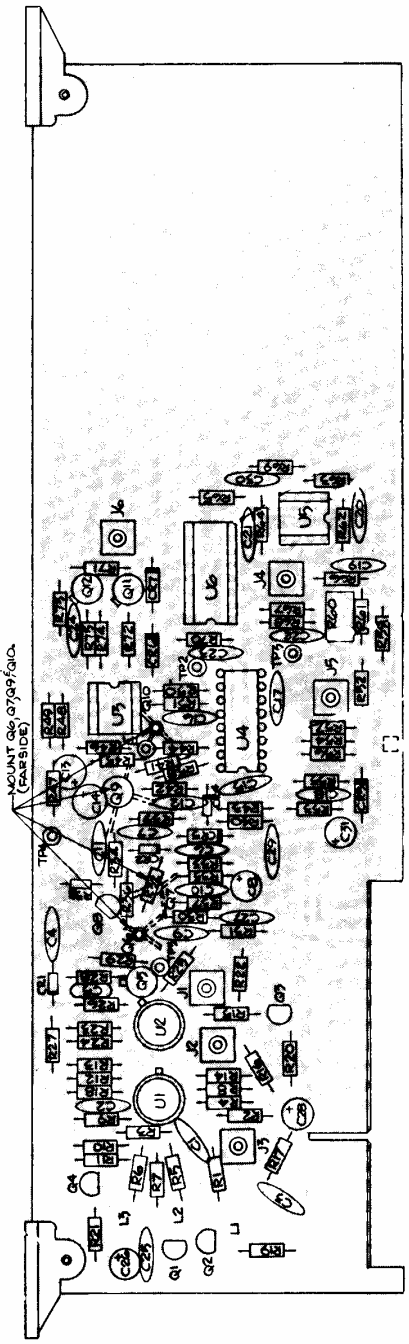
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A106	High Frequency	2020081	1	EIP	34257
C1	Cer, .001μF, 20%, 1KV	2150001	7	5GA - D10	56289
C2	C1				
C3	Cer., .01μF, 20%, 100V	2150003	17	TG - S10	56289
C4	C3				
C5	Mica, 10pF, 5%, 500V	2250001	1	DM15 - 100D	72136
C6	C3				
C7	C3				
C8	Tant, 10μF, 20%, 25V	2300029	3	TAG 20-10/25	72136
C9	C3				
C10	C3				
C11	C1				
C12	C1				
C13	Tant, 47μF, 10%, 16V	2300025	2	TAG 20-47/16	72136
C14	C13				
C15	C1				
C16	C3				
C17	C1				
C18 thru C20	C3				
C21	C1				
C22 thru C25	C3				
C26	C8				
C27	C3				
C28	C8				
C29	C3				
C30	C3				
C31	Tant, 33μF, 20%, 10V	2300015	1	TAG 20-33/10	14433
CR1	General Purpose	2704154	3	IN4154	07263
CR2	CR1				
CR3	Zener, 6.2V	2705234	1	IN5234	07263
CR4	CR1				
CR5	Zener, 5.1V	2705231	1	IN5231	07263
CR6	Hot Carrier	2710004	2	FH1100	07263
CR7	CR6				
Q1	NPN, General Purpose	4704124	1	2N4124	04713
Q2	PNP, General Purpose	4704126	3	2N4126	04713
Q3	Q2				
Q4	Q2				
Q5	PNP, RF	4704959	1	2N4959	04713

A106 HIGH FREQUENCY, continued 2020081-M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
Q6	NPN, RF Switch	4710017	3	MMT3960	04713
Q7	Q6				
Q8	PNP, RF	4710039	1	A8T4261-18	01295
Q9	NPN, RF	4710024	1	BFR90	04713
Q10	Q6				
Q11	RF, Graded	4710011	2	2N5179	04713
Q12	Q11				
R1	Comp, 51, 5%, 1/4 W	4010510	3	RC07GF510J	81349
R2	Comp, 3.9K, 5%, 1/4 W	4010392	1	RC07GF3921	81349
R3	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/1K	24546
R4	Comp, 2K, 5%, 1/4 W	4010202	1	RC07GF202J	81349
R5	Met Ox, S.A.T.(12 ohm NOM)	4130999	5	C4/2%/XX	
R6	R5				
R7	Comp, 220, 5%, 1/4 W	4010221	2	RC07GF221J	81349
R8	Comp, 330, 5%, 1/4 W	4010331	1	RC07GF331J	81349
R9	R3				
R10	Comp, 1K, 5%, 1/4 W	4010102	6	RC07GF102J	81349
R11	R10				
R13	Comp, 3K, 5%, 1/4 W	4010302	3	RC07GF302J	81349
R14	R1				
R15	R12				
R16	R13				
R17	Comp, 5.6K, 5%, 1/4 W	4010596	6	RC07GF596J	81349
R18	Comp, 510, 5%, 1/4 W	4010511	2	RC07GF511J	81349
R19 thru R21	R10				
R22	R1				
R23	R12				
R24	R13				
R25	Met Ox, 2K, 2%, 1/4 W	4130202	1	C4/2%/2K	24546
R26	Met Ox, 68, 2%, 1/4 W	4130680	1	C4/2%/68	24546
R27	R17				
R28	Met Ox, 43, 2%, 1/4 W	4130430	1	C4/2%/43	24546
R29	Met Ox, 100, 2%, 1/4 W	4130101	2	C4/2%/100	24546
R30	Comp, 430, 5%, 1/4 W	4010431	1	RC07GF431J	81349
R31	R17				
R32	Met Ox, 56, 2%, 1/4 W	4130560	2	C4/2%/560	24546
R33	R17				
R34	R32				
R35	Met Ox, 1.5K NOM - S.A.T.	4130999	1	C4/2%/S.A.T.	24546
R36	R17				
R37	R29				
R38	Comp, 82, 5%, 1/8 W	4000820	1	RC05GF820	81349
R39	Comp, 47, 5%, 1/4 W	4010470	1	RC07GF470J	81349

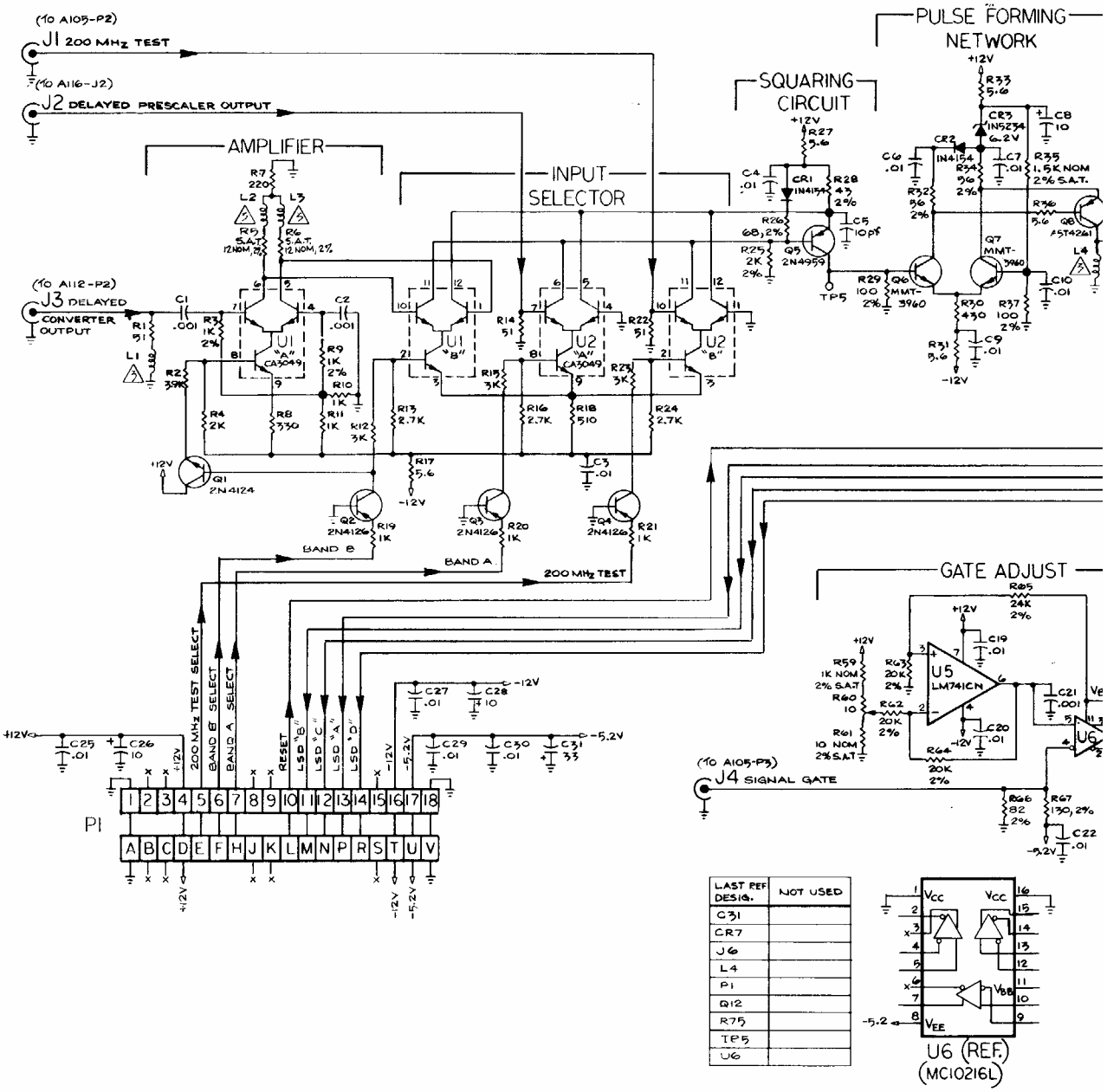
A106 HIGH FREQUENCY, continued 2020081-M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R40	R18				
R41	Comp, 10, 5%, 1/4 W	4010100	1	RC07GF100J	81349
R42	Met Ox, 39, 2%, 1/4 W	4130390	2	C4/2%/390	24546
R43	R17				
R44	R42				
R45	Met Ox, 20K, 2%, 1/4 W	4130203	7	C4/2%/203	24546
R46	R10				
R47	Met Ox, 18, 2%, 1/4 W NOM	4130999	1	C4/2%/S.A.T.	24546
R48	R45				
R49	R3				
R50	R45				
R51	R45				
R52	Comp, 680, 5%, 1/4 W	4010681	1	RC07GF681J	81349
R53	Comp, 1.8K, 5%, 1/4 W	4010182	1	RC07GF182J	81349
R54	Comp, 10K, 5%, 1/4 W	4010103	4	RC07GF103J	81349
R55 thru R57	R54				
R58	Met Ox, 220, 2%, 1/4 W	413221	3	C4/2%/221	24546
R59	Met Ox, 1K, 2%, 1/4 W, NOM	4130999	1	C4/2%/S.A.T.	24546
R60	Variable, Cer., 10 ohm	4250011	1	72XWR10	73138
R61	Met Ox, 10, 2%, 1/4 W, NOM	4130999	1	C4/2%/S.A.T.	24546
R62 thru R64	R45				
R65	Met Ox, 24K,, 2%, 1/4 W	4130243	1	C4/2%/243	24546
R66	Met Ox, 82, 2%, 1/4 W	4130830	1	C4/2%/820	24546
R67	Met Ox, 130, 2%, 1/4 W	4130131	2	C4/2%/131	24546
R68	R58				
R69	R58				
R70	R7				
R71	Comp, 150, 5%, 1/4 W	4010151	1	RC07GF151J	81349
R72	Met Ox, 680, 2%, 1/4 W	4130681	1	C4/2%/681	24546
R73	R67				
R74	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/472	24546
R75	Met Ox, 560, 2%, 1/4 W	4130561	1	C4/2%/561	24546
U1	Lin, Dual Diff. Amplifier	3043049	2	CA3049T	
U2	U1				
U3	Lin, Op Amplifier	3040741	1	27014	
U4	Dacade Counter, UHF/BCD	3010637	1	0000C	
U4	(Attenuate) High Speed Divider	3018636	Ref	0000C	
U5	U3				
U6	Triple Line Receiver	3110216	1	04713	



2020081 - M

Figure 106-1. High Frequency Component Locator



LAST REF DESIG.	NOT USED
C31	
CR7	
J6	
L4	
P1	
Q12	
R75	
TP5	
U6	

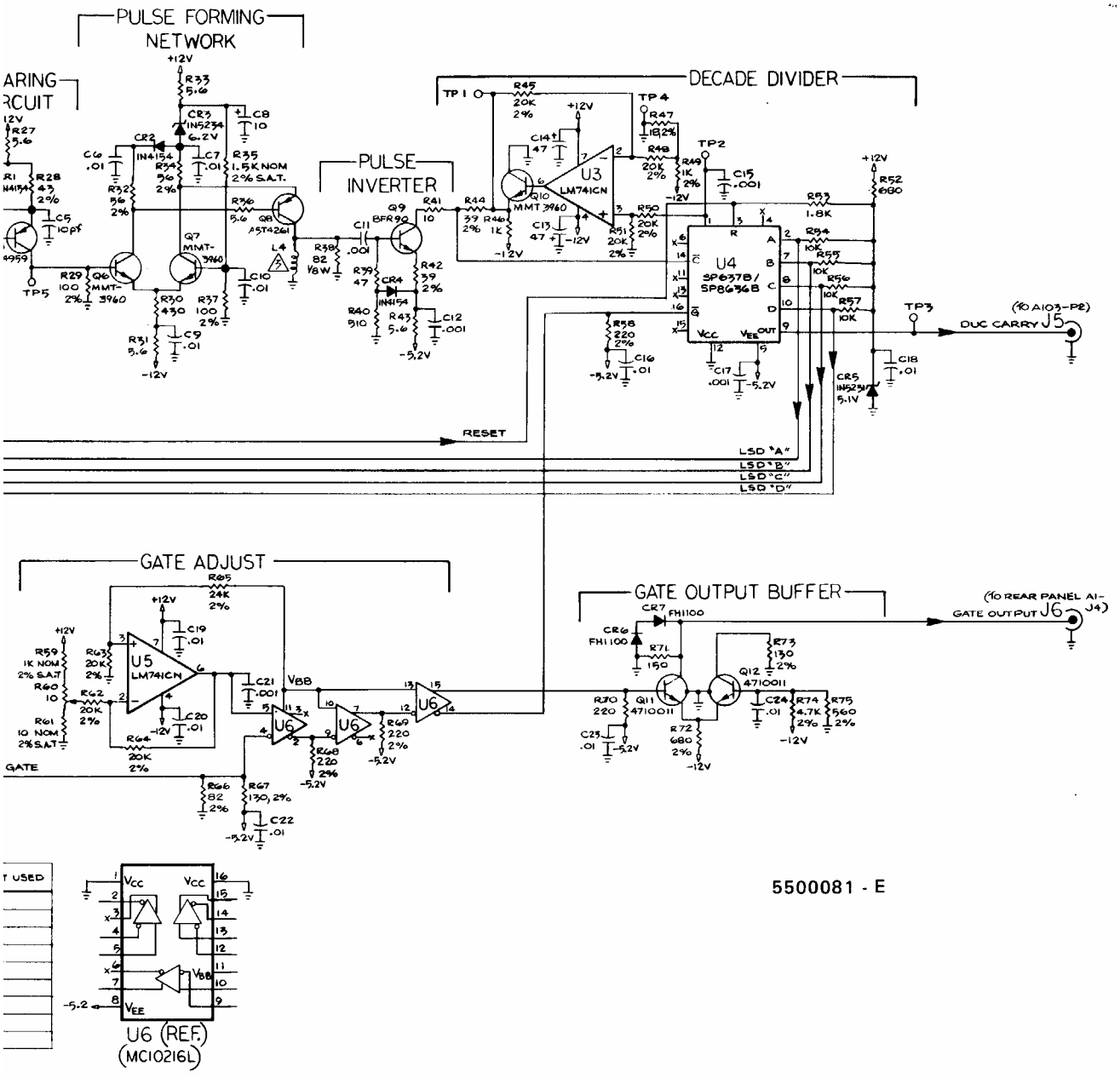


Figure 106-2. High Frequency Schematic

A107
POWER SUPPLY
(2020077)

The Power Supply furnishes all basic operating voltages required by the counter. The supply consists of two assembly groups:

(1) PC board A107 containing the rectifiers, filter capacitors, and regulator circuitry.

(2) Chassis mounted components (A1-) consisting of the power transformer (A1T1), primary wiring, POWER INPUT module (containing the fuse, voltage changing PCB, and power input connector), and the front panel POWER switch.

CIRCUIT DESCRIPTION

The basic voltages required by the counter are: unregulated +18 Vdc, regulated +12 Vdc, +5 Vdc, -12UDC and -5.2 Vdc.

All the regulated voltages are produced by full wave rectifier and series regulator circuits. The +18V unregulated voltage is also the input voltage for the +12V regulator.

Each of the four regulator circuits contains an integrated circuit voltage regulator with current foldback capability, protective diodes, and provision for adjustment of the required output voltage.

The type of IC used in both the +12V and +5V regulators is an LM 305. This IC contains an internal temperature compensated voltage reference, as well as the necessary circuits to provide gain and current foldback limiting. The foldback current limit control resistors in the +5V supply (for example), are R11, R12, and R13.

The negative supplies utilize an LM 304 as the basic IC regulator. This IC also contains an internal temperature compensated reference. To implement this reference an external pre-regulator is required. In the -12V circuit (for example), the pre-regulator includes R22, R25, and CR9. Current foldback limiting uses internal IC circuitry in addition to R17, R18, R19 and Q5.

A107 POWER SUPPLY

2020077 - Y

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A107	Power Supply	2020077	1	EIP	34257
C1	Elec, 9500μF, -10 + 75%, 25V	2200016	2	3110HA952U025	80031
C2	Tant, 10μF, 20%, 25V	2300029	4	TAG 20-10/25	14433
C3	Mica, 47pF, 5%, 500V	2250017	1	DM15-470J	72136
C4	C2				
C5	Elec, 44,000μF, -10 + 75%, 15V	2200018	1	3110JB443U015	80031
C6	C2				
C7	Mica, 200pF, 5%, 500V	2250009	1	DM15-200J	72136
C8	Tant, 47μF, 10%, 16V	2300025	1	TAG 20-47/16	14433
C9	Tant, 33μF, 10%, 20V	2300023	2	TAG 20-33/20	14433
C10	Tant, 1.0μF, 10%, 35V	2300008	2	TAG 20-1.0/35	14433
C11	Cer, .001μF, 20%, 1KV	2150001	2	5GA - D10	56289
C12	C1				
C13	C9				
C14	C10				
C15	C11				
C16	C2				
C17	Elec, 10,000μF, -10 + 75%, 15V	2200025	1	3050JP103U015	80031
CR1	Power Rectifier	2704001	8	IN4001	04713
CR2 thru CR4	CR1				
CR5	Bridge Rectifier	2710028	1	MDA990-1	04713
CR6	Bridge Rectifier	2710029	1	MDA970-1	04713
CR7	CR1				
CR8	CR1				
CR9	Zener, 12V	2720963	2	IN963A	04713
Q1	NPNP, Power	4710002	4	MJE520	04713
Q2	NPN, Power	4710001	3	MJE3055	04713
Q3	Q1				
Q4	NPN, Power	4705989	1	2N5989	04713
Q5	PNP, General Purpose	4704126	2	2N4126	04713
Q6	Q1				
Q7	Q2				
Q8	Q5				
Q9	Q1				
Q10	Q2				
R1	Comp, 68, 5%, 1/4 W	4010680	4	RC07GF680J	81349
R2	Met Ox, 36, 2%, 1/4 W	4130360	1	C4/2%/36	24546
R3	Met Ox, 820, 2%, 1/4 W	4130821	2	C4/2%/820	24546
R4	Wire Wound, .5, 3%, 3W	4110004	2	RS-2B	91637
R5	R3				

A107 POWER SUPPLY, continued 2020077 - Y

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R6	Met Film, 14.7K, 1%, 8W	4061472	1	RN55D1472F	81349
R7	Var, Cer, 500 ohm	4250009	3	72XWR500	73138
R8	Met Film, 2.26K, 1%, 1/8 W	4062261	1	RN55D2261F	81349
R9	Comp, 43, 5%, 1/4 W	4020430	1	RC20GF430J	81349
R10	R1				
R11	Met Ox, 20, 2%, 1/4 W	4130200	1	C4/2%/20	24546
R12	Met Ox, 100, 2%, 1/4 W	4130101	1	C4/2%/100	24546
R13	Wire Wound, 0.15, 3%, 5 W	4110013	1	RS - 5	91637
R14	Met Film, 5.62K, 1%, 1/8 W	4065621	1	RN55D5621F	81349
R15	R7				
R16	Met Film, 2.87K, 1%, 1/8 W	4062871	1	RN55D2871F	81349
R17	Met Ox, 12K, 2%, 1/4 W	4130123	1	C4/2%/12K	24546
R18	Wire Wound, .66, 3%, 4W	4110012	1	RS-2	91637
R19	Met Ox, 910, 2%, 1/4 W	4130911	2	C4/2%/910	24546
R20	Met Ox, 5.6K, 2%, 1/4 W, NOM	4130999	1	C4/2%/S.A.T.	24546
R21	Var, Cer, 1K	4250003	1	72XWR1K	73138
R22	Met Film 2.43K, 1%, 1/8 W	4062431	3	RN55D2431F	81349
R23	R1				
R24	Comp, 100, 5%, 1/4 W	4010101	2	RC07GF101J	81349
R25	Comp, 1K, 5%, 1/4 W	4010102	2	RC07GF102J	81349
R26	Met Os, 5.1K, 2%, 1/4 W	4130512	1	C4/2%/5.1K	24546
R27	R4				
R28	R19				
R29	Comp, 910, 5%, 1/4 W	4010911	1	RC07GF911J	81349
R30	R22				
R31	R7				
R32	R22				
R33	R1				
R34	R24				
R35	R25				
U1	Voltage Regulator	3040305	2	LM305	27014
U2	U1				
U3	Voltage Regulator	3040304	2	LM304	27014
U4	U3				
	Heat Sink (Long)	5210017-02	1		

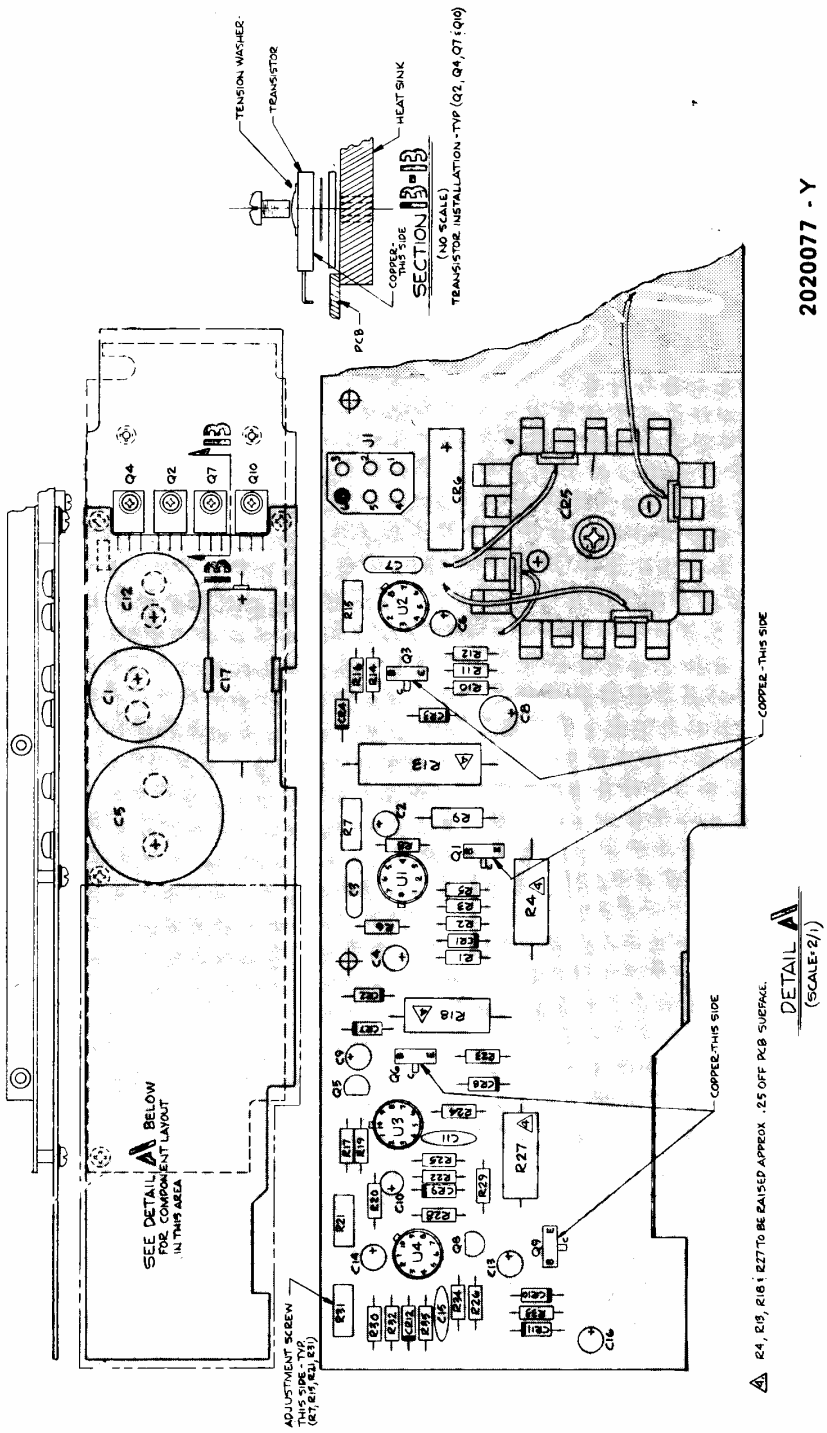
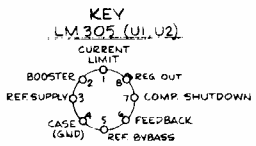
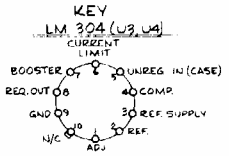
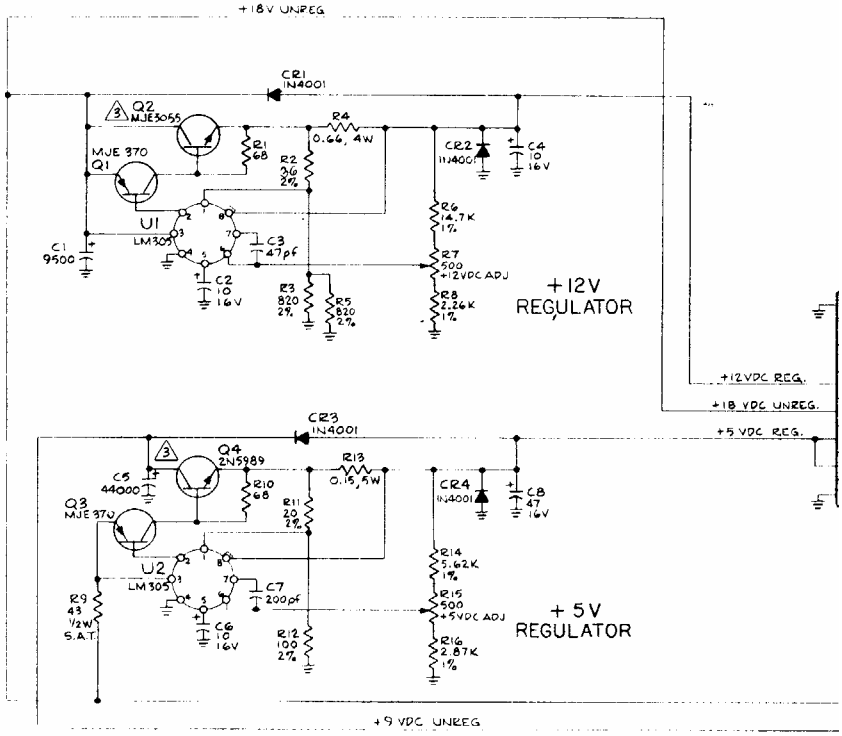
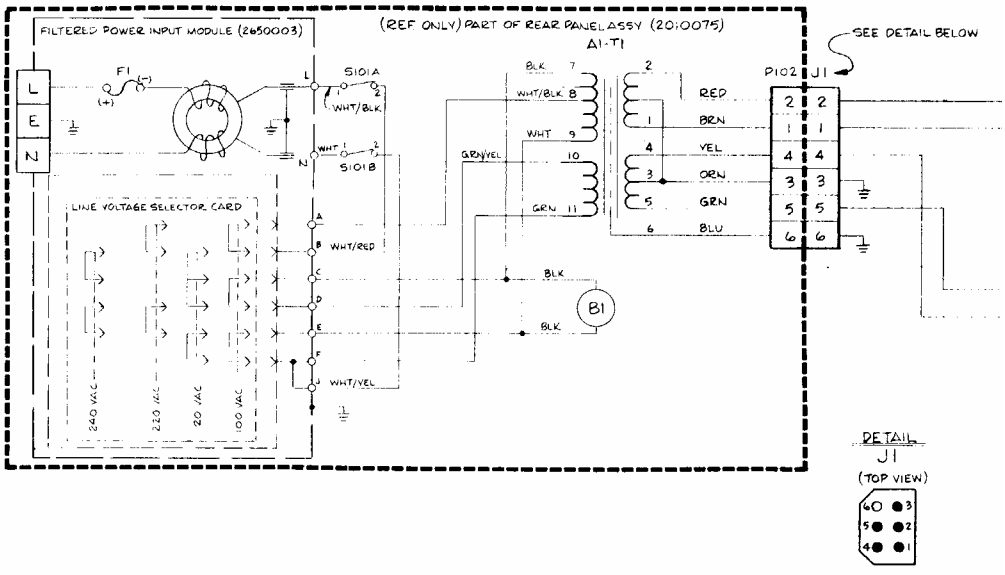


Figure 107-1. Power Supply Component Locator


KEY
LM 305 (U1, U2)
CURRENT LIMIT
BOOSTER
REG. OUT
REF. SUPPLY
COMP. SHUTDOWN
CASE (GND)
FEEDBACK
REF. BYPASS


KEY
LM 304 (U3, U4)
CURRENT LIMIT
BOOSTER
UNREG. IN (CASE)
REG. OUT
COMP.
GND
REF. SUPPLY
N/C
REF.
ADJ


+18V UNREG.
CR1 IN4001
Q2 MJE3055
MJE 370 Q1
R4 0.66, 4W
R1 68
R2 36 2%
CR2 IN4001
C4 10 16V
R6 14.7K 1%
U1 LM309
C3 47pf
C1 9500
C2 10 16V
R7 500 +12VDC ADJ
R3 820 2%
R5 820 2%
R8 2.26K 1%
+12V REGULATOR
+12VDC REG.
+18 VDC UNREG.
+5 VDC REG.
CR3 IN4001
Q4 2N5989
C5 44000
R13 0.15, 5W
R10 68
R11 20 2%
CR4 IN4001
C8 47 16V
Q3 MJE 370
U2 LM305
R14 5.62K 1%
R15 500 +5VDC ADJ
C7 200pf
R9 43 1/2W S.A.T.
C6 10 16V
R12 100 2%
R16 2.87K 1%
+5 V REGULATOR
+9 VDC UNREG.


FILTERED POWER INPUT MODULE (2650003)
(REF ONLY) PART OF REAR PANEL ASSY (20:0075)
A1-T1
SEE DETAIL BELOW
L
E
N
F1
S101A
S101B
WHT/BLK
WHT
LINE VOLTAGE SELECTOR CARD
240 VAC
220 VAC
120 VAC
100 VAC
WHT/RED
WHT/VEL
BLK
GRN/YEL
GRN
B1
P102
J1
RED
BRN
YEL
ORN
GRN
BLU

DETAIL
J1
(TOP VIEW)

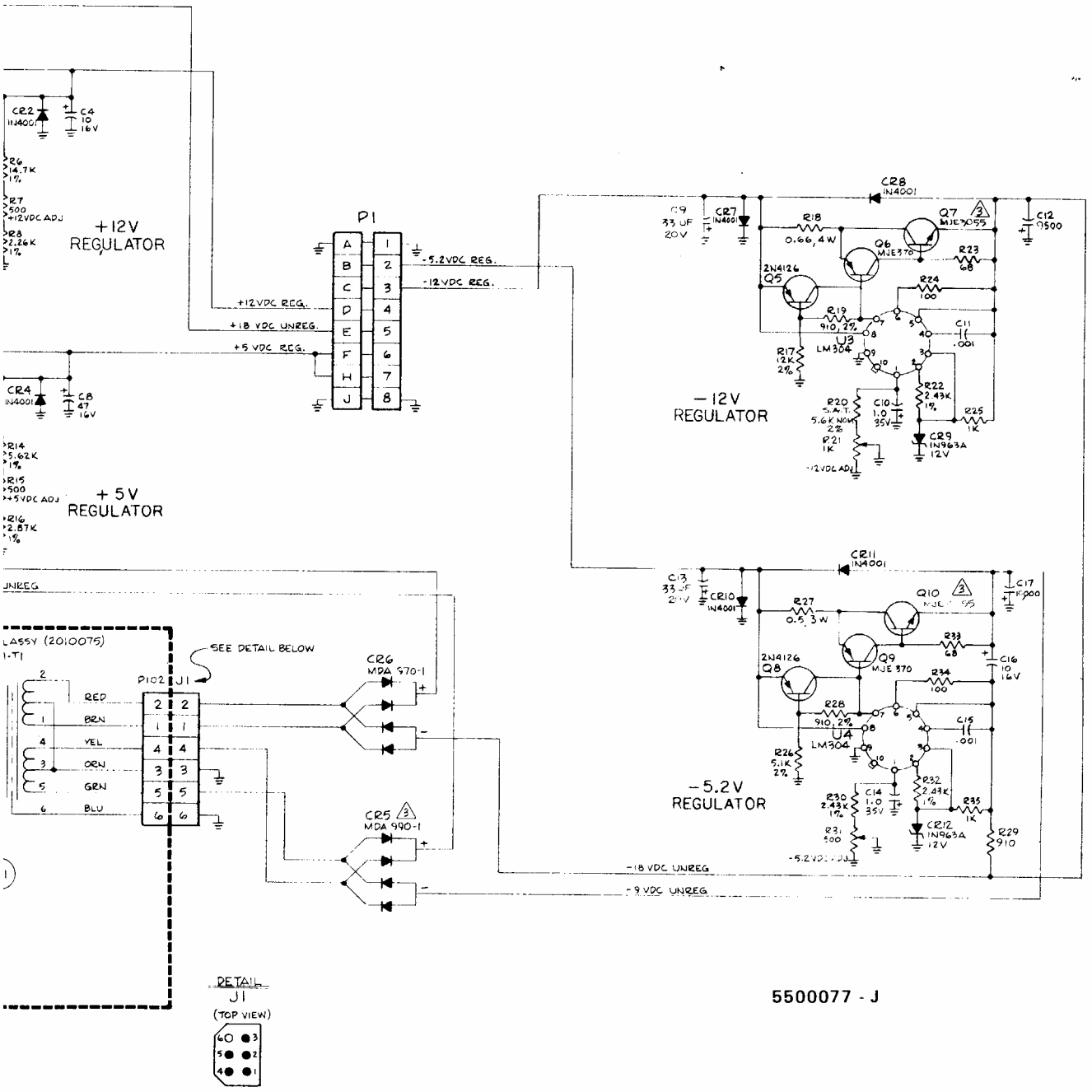


Figure 107-2. Power Supply Schematic

A108
REFERENCE OSCILLATOR BUFFER
(2020078)

A room temperature, crystal controlled oscillator (RTO) is used as the basic reference against which all input signals are compared. An additional temperature-compensated crystal oscillator (TCXO) is available as Option P1, which allows the user to select a higher level of precision compatible with measurement requirements.

CIRCUIT DESCRIPTION

The signal from the oscillator is either a square wave from the RTO, or a sine wave from the optional TCXO. This waveform is converted to a positive-going square wave at J1 by a linear amplifier (Q1), current switch (Q2, Q3), and an output current driver (Q4).

The outputs appearing at P1 pins 6 and 14, are processed by a linear, low gain amplifier pair (Q5 and Q6), and two identical line driver circuits Q7-Q10, and Q11-Q14). Low gain, common emitter input stages (Q7, Q11), are followed by emitter followers (Q8, Q12), which drive push-pull emitter follower output pairs (Q9, Q10, and Q13, Q14).

PAGE LEFT BLANK INTENTIONALLY

A108 REFERENCE OSCILLATOR BUFFER

-2020078 - M

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A108	Reference Oscillator Buffer	2020078	1	EIP	34257
C1	Cer, .01μF, 20%, 100V	2150003	29	TG - S10	56289
C2	C1				
C3	Mica, 100pF, 5%, 500V	2250002	1	DM-15-101J	72136
C4	Cer, no NOM value	2160000	1	301000C0 S.A.T.	
C5	Trim, 2-8pF, 250V	2350021	1	10S-T-24-2/8	
C6 thru C10	C1				
C11	Not Used				
C12 thru C21	C1				
C22	Mica, 33pF, 5%, 500V, NOM	2250014	1	DM15CD330J0 S.A.T	72136
C23 thru C31	C1				
C32	Tant, 33μF, 20%, 10V	2300015	1	TAG 20-33/10	14433
C33	C1				
C34	Tant, 10μF, 20%, 25V	2300029	2	TAG 20-10/25	14433
C35	C1				
C36	C1				
C37	C34				
CR1 CR2 thru CR4	General Purpose	2704154	4	IN4154	07263
	CR1				
Q1	NPN	4703563	8	2N3563	07263
Q2	Q1				
Q3	Q1				
Q4	PNP, RF	4710010	3	MPS-H81	04713
Q5	Q1				
Q6	PNP, General Purpose	4704126	1	2N4126	04713
Q7	PNP, RF Graded, 2N5179-RED	4710011	2	4705179	34257
Q8	Q1				
Q9	Q1				
Q10	Q4				
Q11	Q7				
Q12	Q1				
Q13	Q1				
Q14	Q4				

A108 REFERENCE OSCILLATOR BUFFER, continued

2020078 - M

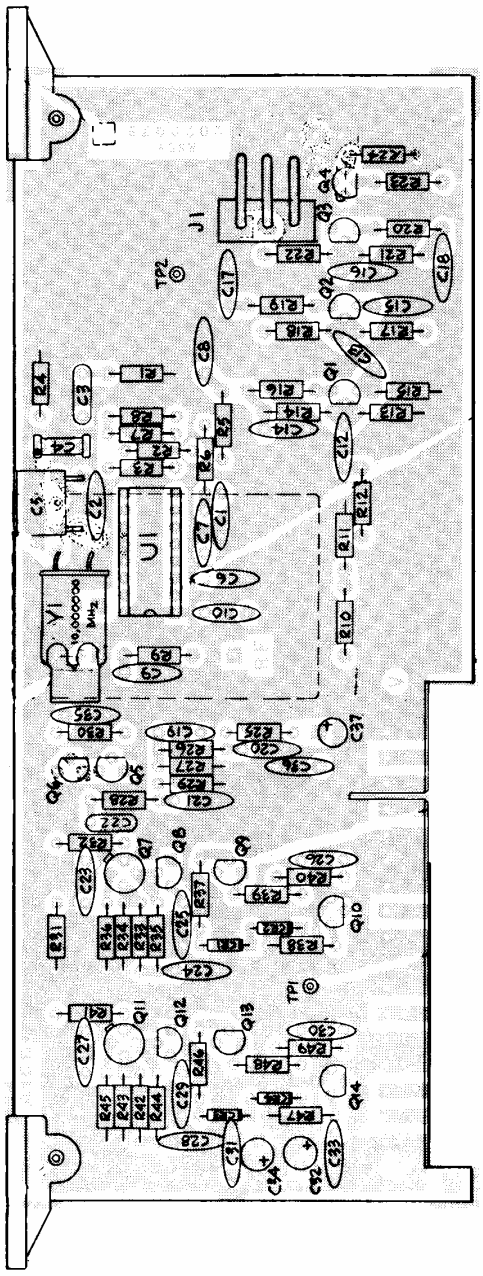
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1	Met Ox, S.A.T.	4130999	1	C4/2%/S.A.T.	24546
R2	Met Ox, 1K, 2%, 1/4 W	4130102	4	C4/2%/1K	24546
R3	R2				
R4	Comp, 1M, 5%, 1/4 W	4010105	1	RC07GF105J	81349
R5	Comp, 3.3K, 5%, 1/4 W	4010332	2	RC07GF332J	81349
R6	R5				
R7	R2				
R8	R2				
R9	Comp, 1K, 5%, 1/4 W	4010102	1	RC07GF102J	81349
R10	Comp, 5.6, 5%, 1/4 W	4010596	1	RC07GF596, S.A.T.	81349
R11	Comp, S.A.T.	4010XXX	1	RC07GFXXX, S.A.T.	81349
R12	Comp, 10, 5%, 1/4 W	4010100	6	RC07GFX00J	81349
R13	Met Ox, 8.2K, 2%, 1/4 W	4130822	5	C4/2%/8.2K	24546
R14	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/3.9K	24546
R15	Met Ox, 680, 2%, 1/4 W	4130681	3	C4/2%/680	24546
R16	Met Ox, 390, 2%, 1/4 W	4130391	1	C4/2%/390	24546
R17	Met Ox, 9.1K, 2%, 1/4 W	4130912	2	C4/2%/912	24546
R18	R13				
R19	Met Ox, 750, 2%, 1/4 W	4130751	1	C4/2%/751	24546
R20	Met Ox, 180, 2%, 1/4 W	4130181	1	C4/2%/181	24546
R21	R17				
R22	R13				
R23	Met Ox, 27, 2%, 1/4 W	4130270	1	C4/2%/27	24546
R24	Met Ox, 300, 2%, 1/4 W	4130301	1	C4/2%/301	24546
R25	R12				
R26*	Met Ox, 11K, 2%, 1/4 W	4130113	1	C4/2%/113	24546
R27*	Met Ox, 1.3K, 2%, 1/4 W	4130132	1	C4/2%/1.3K	24546
R28	Met Ox, 620, 2%, 1/4 W	4130621	1	C4/2%/620	24546
R29	Met Ox, 100, 2%, 1/4 W	4130101	1	C4/2%/100	24546
R30	Met Ox, 430, 2%, 1/4 W	4130431	1	C4/2%/431	24546
R31	Met Ox, 910, 2%, 1/4 W	4130911	1	C4/2%/911	24546
R32	R12				
R33	R13				
R34	Met Ox, 4.3K, 2%, 1/4 W	4130432	2	C4/2%/4.3K	24546
R35	R15				
R36	Met Ox, 560, 2%, 1/4 W	4130561	2	C4/2%/560	24546
R37	R12				
R38	Met Ox, 1.1K, 2%, 1/4 W	4130112	2	C4/2%/1.1K	24546
R39	Met Ox, 5.1, 5%, 1/4 W	4130591	4	RC07GF591J	24546
R40	R39				
R41	R12				
R42	R13				
R43	R34				
R44	R15				
R45	R36				

A108 REFERENCE OSCILLATOR BUFFER

2020078 - M

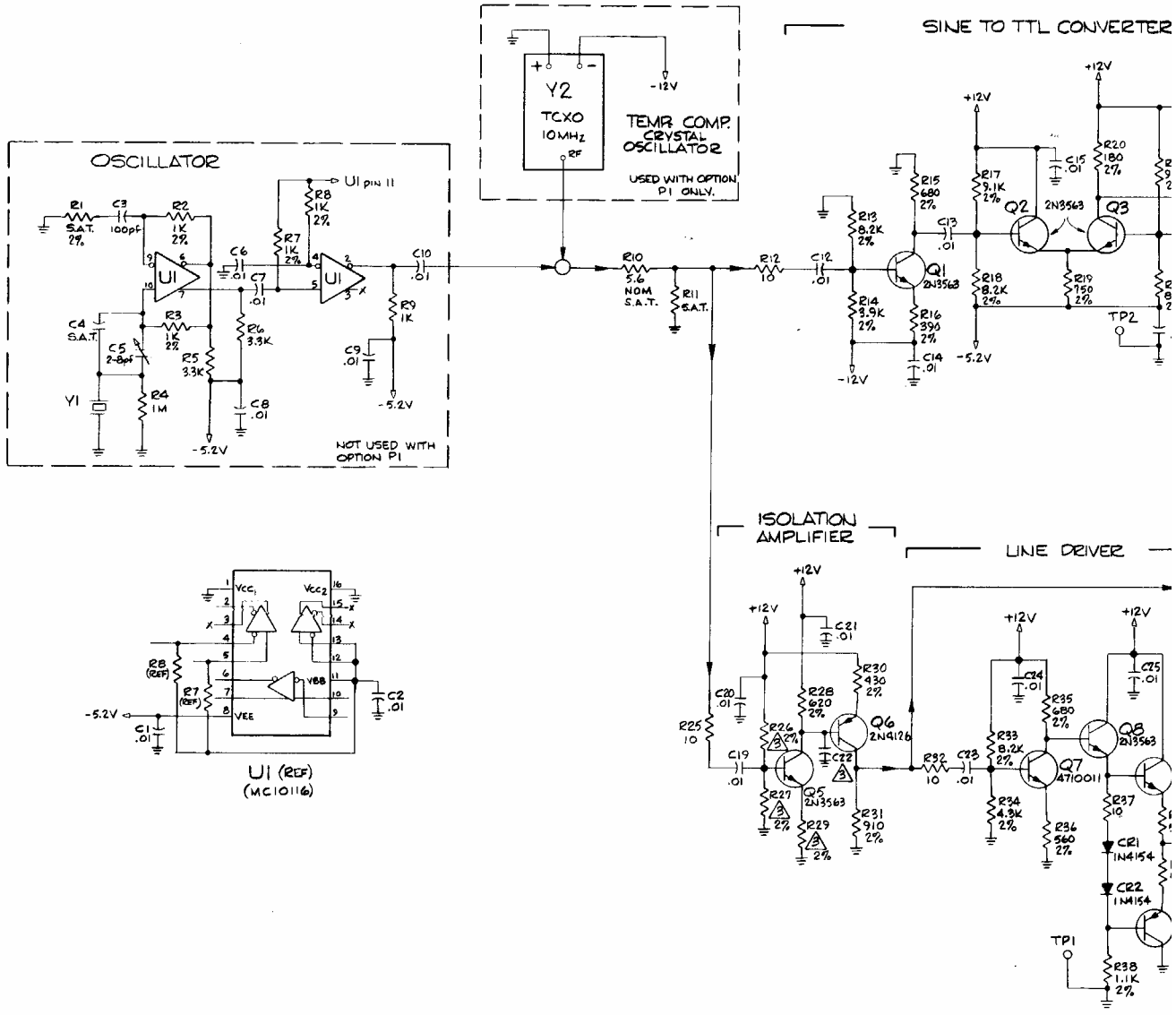
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R46	R12				
R47	R38				
R48	R39				
U1	Triple Line Receiver	3110116	1	MC10116P	04731
Y1	Crystal, 10Hz	2030011	1	A187DED-30	00809
Y2*	TCXO	2030002	1	EIP	34257

* Indicates Option P1 TCXO values



2020078 - M

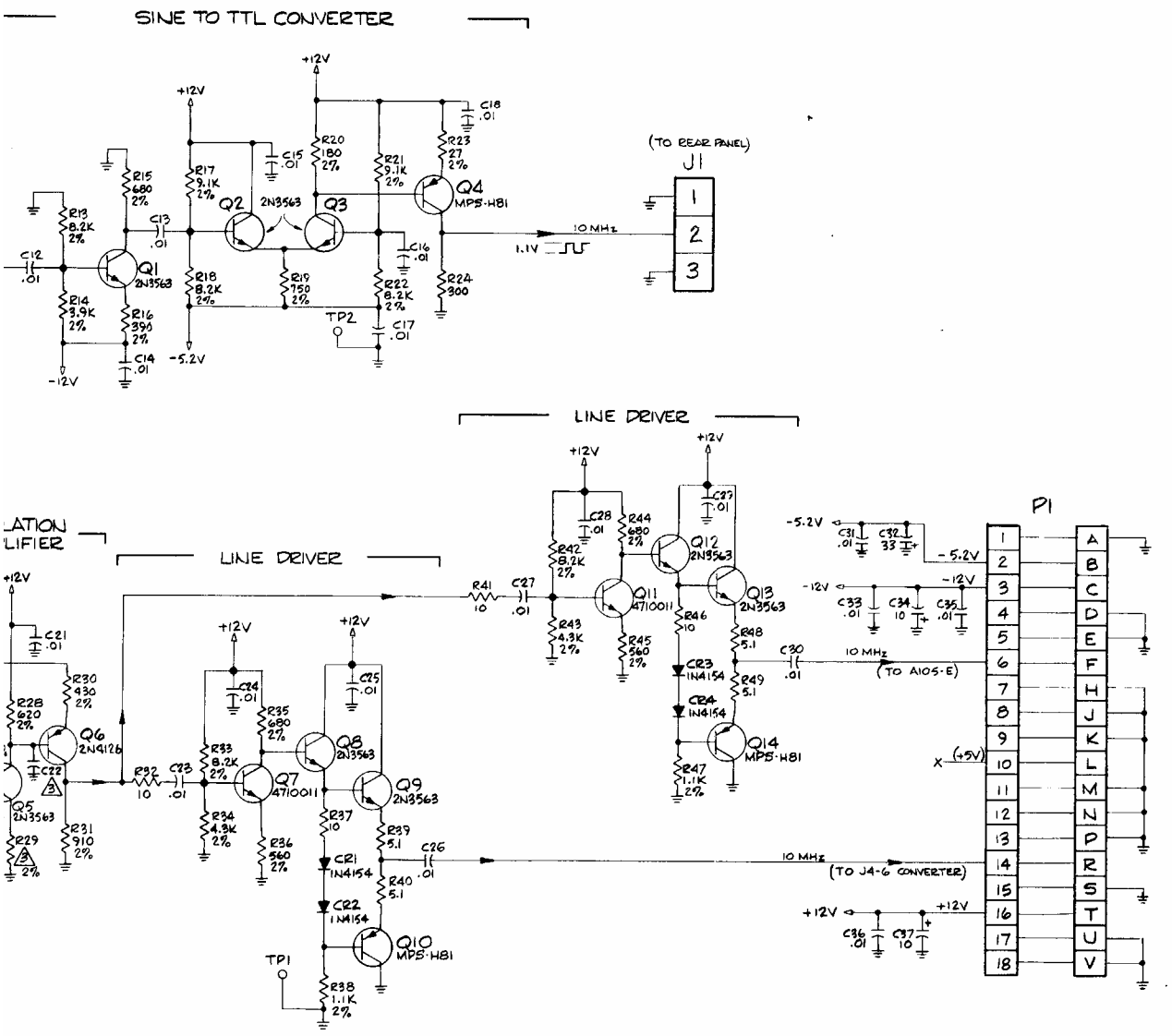
Figure 108-1. Reference Oscillator Buffer Component Locator



REF DESIG.	-01 STD (RM. TEMP OSC.)	-02 OPT P1 (TCXO)
R26	11K	9.1K
R27	1.3K	2.2K
R29	100	360
C22	33 pf. S.A.T.	NOT USED

LAST REF DESIG. USED	NOT USED
C37	C11
CR4	
J1	
Q14	
R49	
U1	
Y2	
TP2	

3 COMPONENT VALUES CHANGE WHEN TCXO OPTION P1 IS USED. SEE TABLE FOR CORRECT COMPONENT VALUE FOR EACH APPLICATION



-02 OPT P1 (TCXO)
9.1K
2.2K
360
NOT USED

LAST REF DESIG. USED	NOT USED
C37	C11
CR4	
J1	
Q14	
R49	
U1	
Y2	
TP2	

5500078 - F

Figure 108-2. Reference Oscillator Buffer Schematic

A110
DISPLAY
(2020080)

Display board A110 contains seven LED numerical display units mounted side-by-side, grouped into a 2-digit GHz section, and a 5-digit MHz section. The MHz section also contains an LED decimal point between the second and third least-significant-digits (decimal point extinguishes when the two least-significant-digits are blanked by the front panel RESOLUTION switches). All drive signals for the display are obtained from the Count Chain Control.

The digit displays are 7-segment LED's, with the anodes of all segments of each digit tied together. When the anode is at a positive voltage, grounding any cathode through its associated resistor illuminates that segment.

In this multiplexed system, the anode supply voltage is applied in pulses (through anode drivers), which are synchronized with the cathode data to determine which segment shall light. The segment drive is applied directly to all display digits. Corresponding cathode segments are all tied together in groups of seven.

The LED digits each use a single transistor driver. The drivers saturate when turned on, applying a voltage almost equal to the supply voltage for the display. This voltage is variable (by A102R35) for display brightness adjustment.

Four display lamps are included on this assembly, which illuminate to indicate GATE operation, input signal LEVEL, LOCK, and REMOTE operation (Option P4).

A110 DISPLAY

2020080 - F

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A110	Display	2020080	1	EIP	34257
DS1 thru DS7	Numeric Indicator	2800004	7	5082-7730	28480
DS8	LED, Red	2800001	1	MV5021	50522
DS9 thru DS11	LED, Green	2800008	3	MV5253	50522
DS12	LED, Yellow	2800014	1	MV5353	50522
R1 thru R5	Comp, 150, 5%, 1/4 W	4010151	5	RC07GF151J	81349

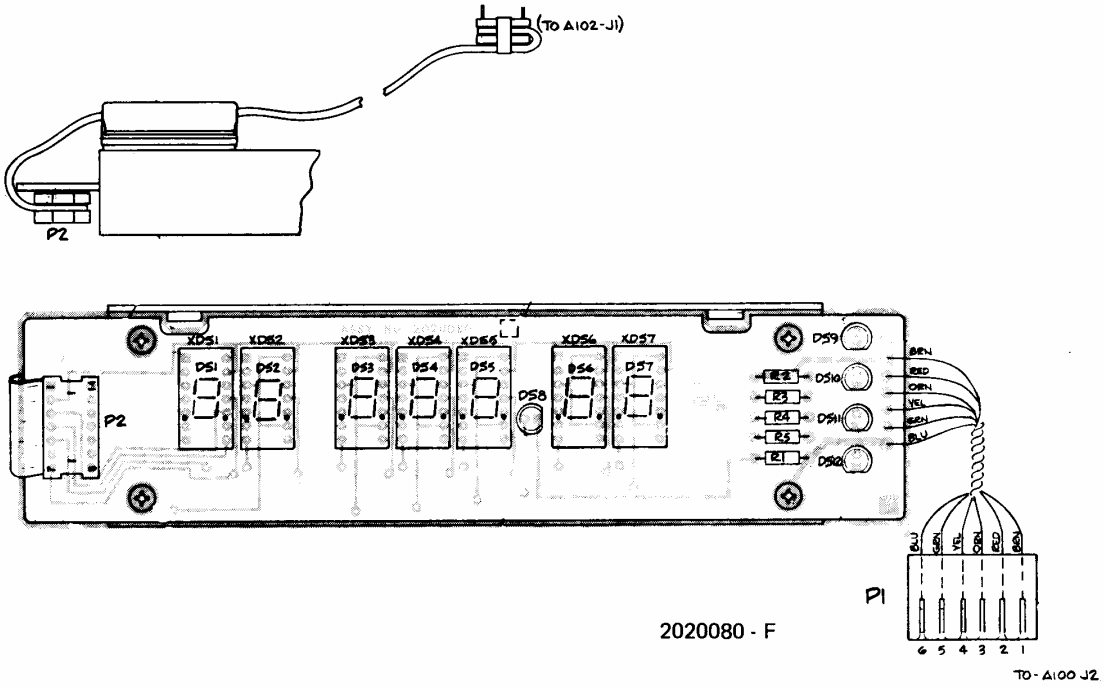
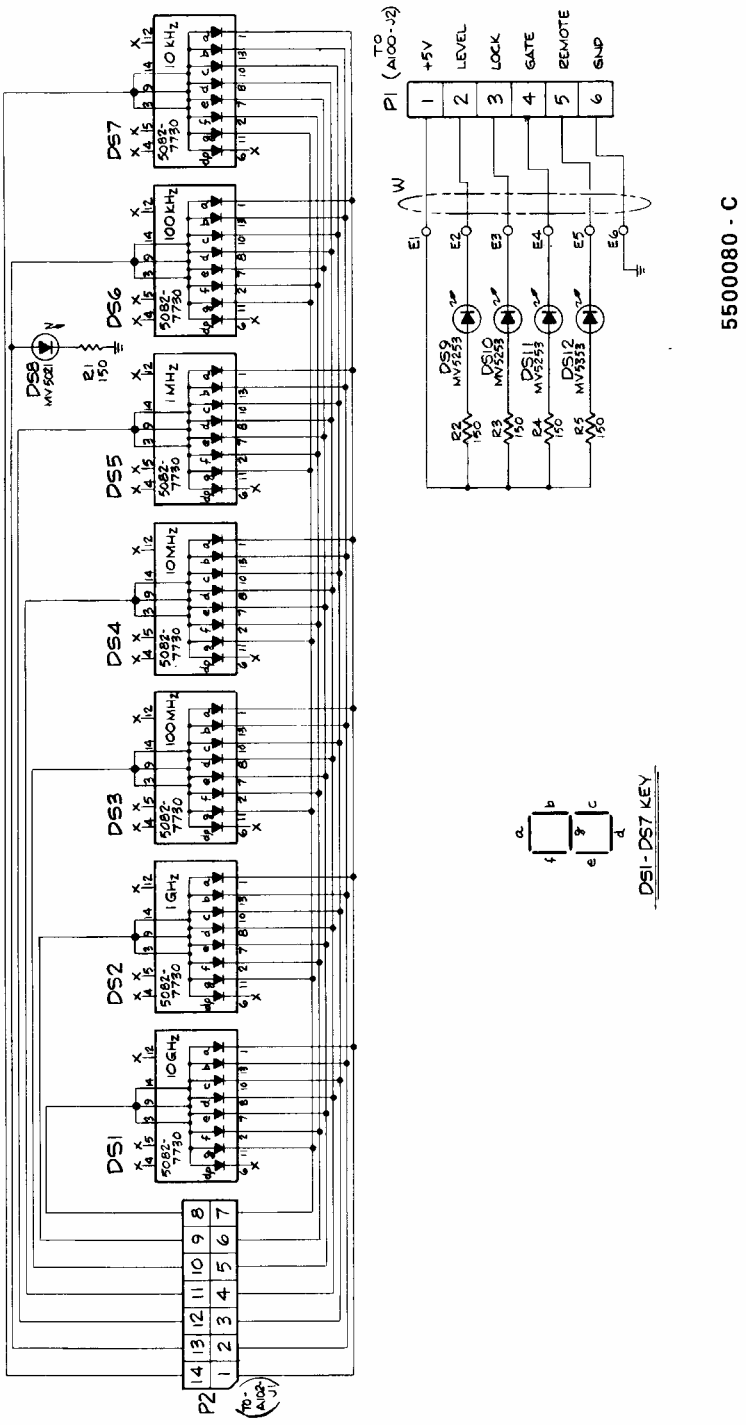


Figure 110-1. Display Component Locator



5500080 - C

Figure 110-2. Display Schematic

A200
CONVERTER INTERCONNECT
(2020090)

FUNCTIONAL DESCRIPTION NOT REQUIRED

A200 CONVERTER INTERCONNECT

2020090 - G

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.
A200	Converter Interconnect	2020090	1	EIP
J1	PC Wafer, 4 pin ML	2620014	1	09-60-1041
J2	PC Wafer, 9 pin ML	2620042	1	09-60-1091
P1	Harness Assy	2040068	1	EIP
P2	Co-ax Cable Assy	2040095	1	EIP
P3	Co-ax Cable Assy	2040096	1	EIP
P4	Co-ax Cable Assy	2040097	1	EIP
P5	Co-ax Cable Assy	2040098	1	EIP
P6	Co-ax Cable	2040099	1	EIP

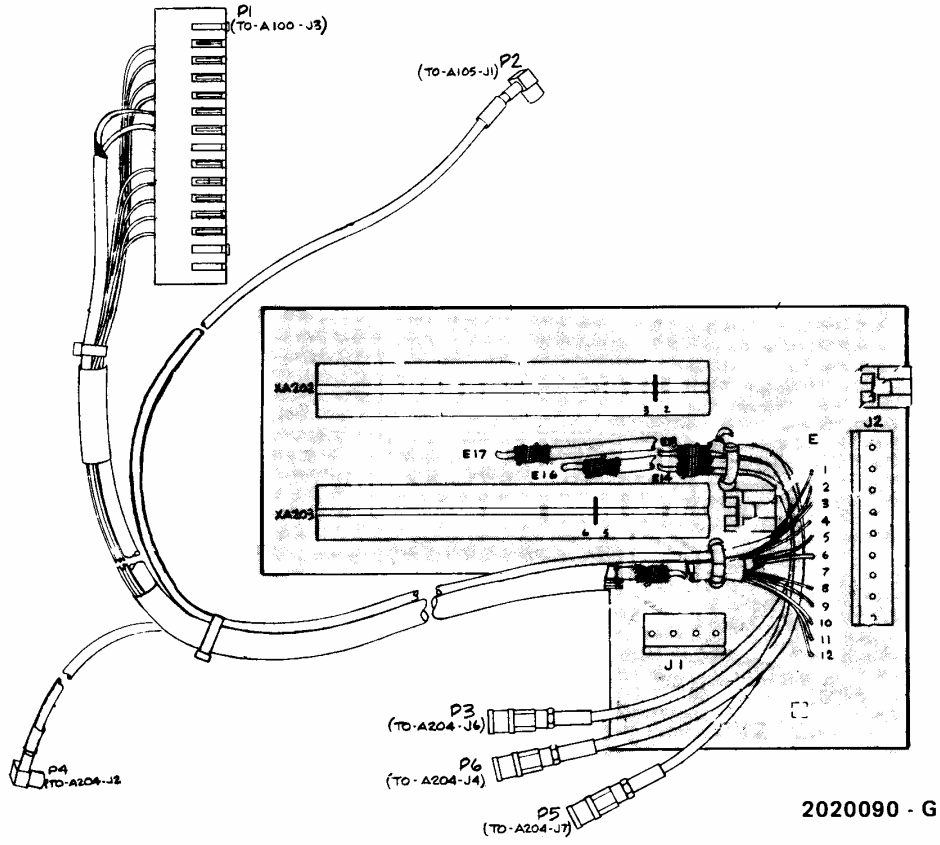
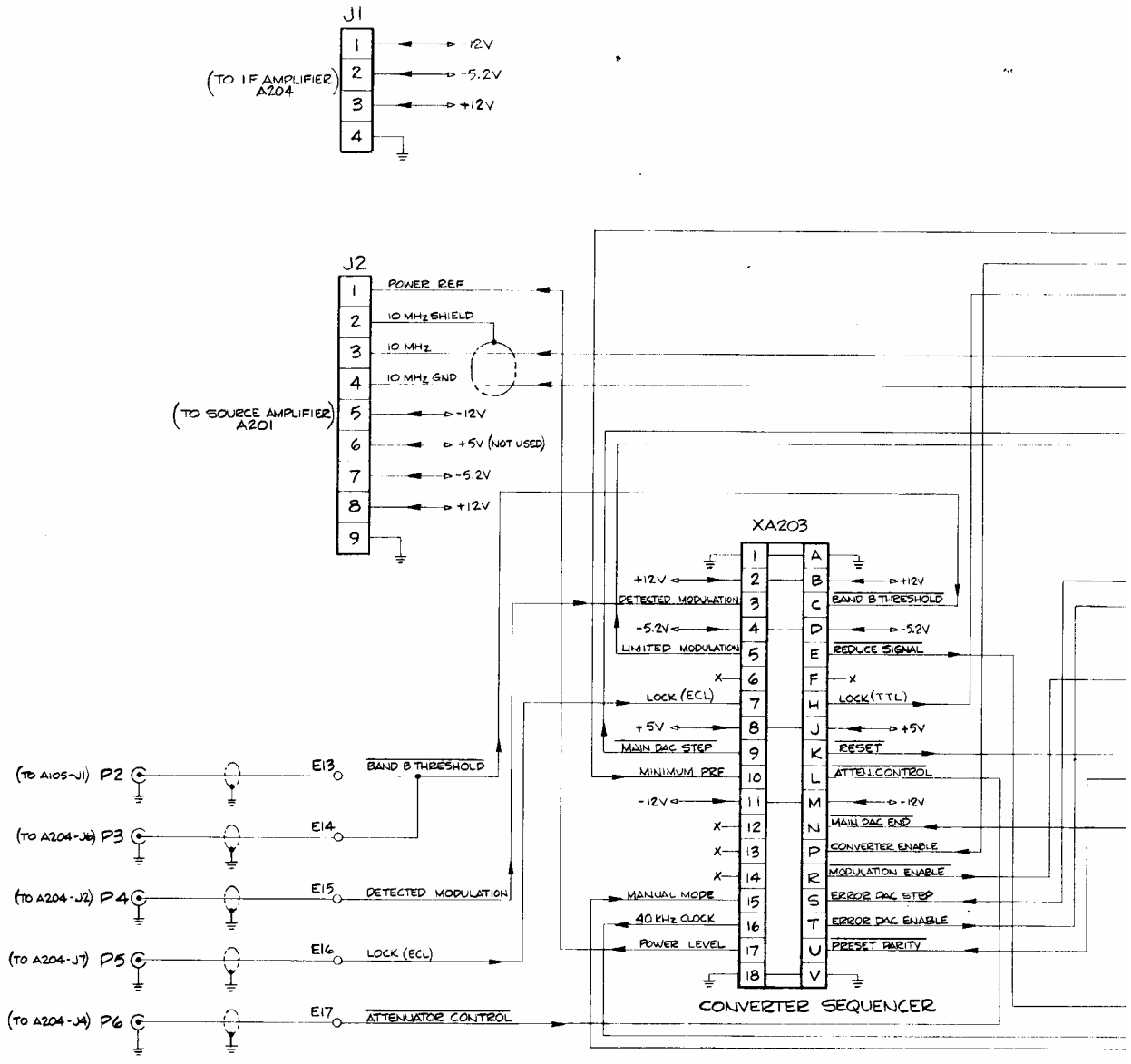
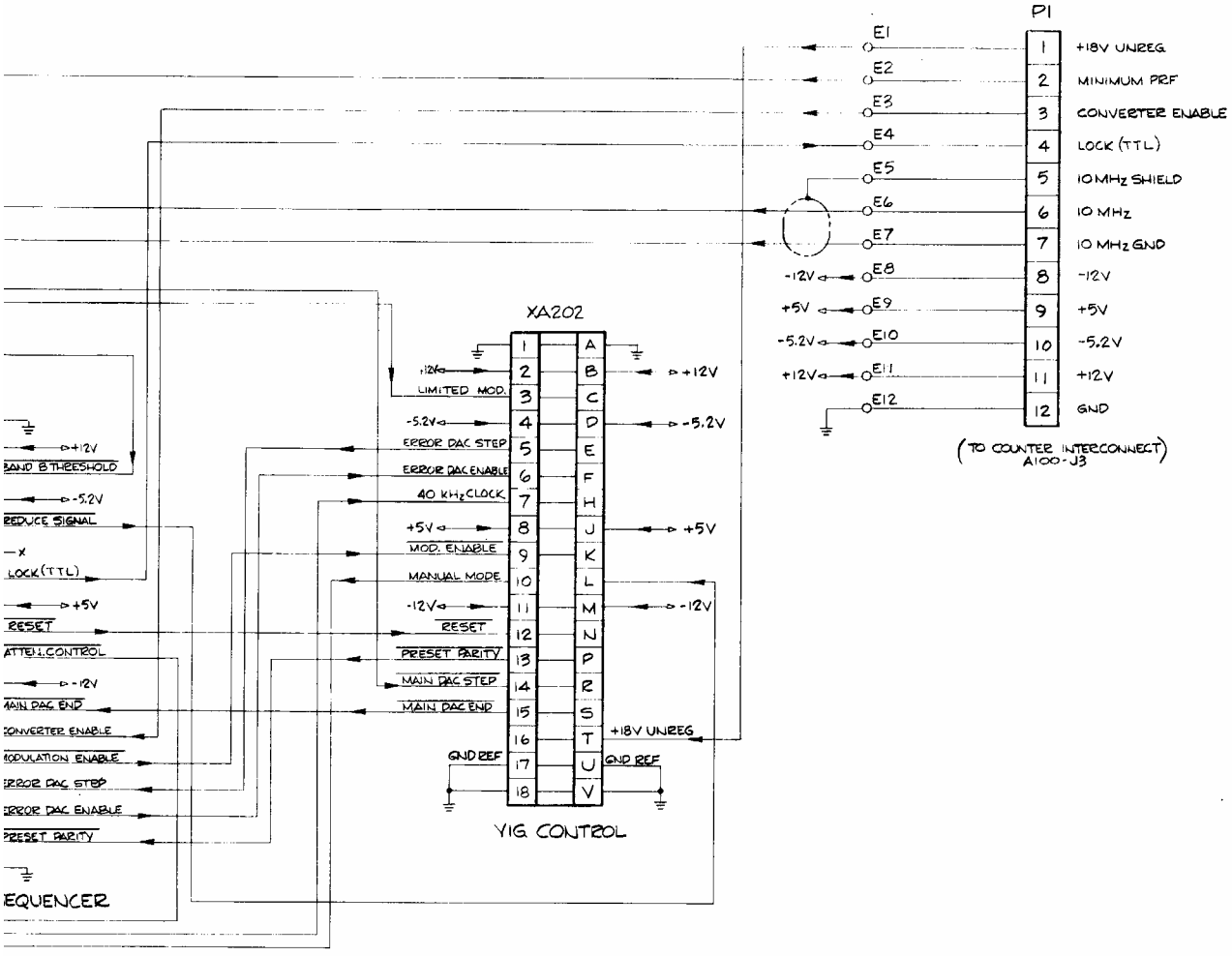


Figure 200-1. Converter Interconnect Component Locator


J1
(TO IF AMPLIFIER A204)
1
2
3
4
-12V
-5.2V
+12V
J2
(TO SOURCE AMPLIFIER A201)
1 POWER REF
2 10 MHz SHIELD
3 10 MHz
4 10 MHz GND
5 -12V
6 +5V (NOT USED)
7 -5.2V
8 +12V
9
XA203
+12V
DETECTED MODULATION
-5.2V
LIMITED MODULATION
X
LOCK (ECL)
+5V
MAIN DAC STEP
MINIMUM PRF
-12V
X
X
X
MANUAL MODE
40 KHz CLOCK
POWER LEVEL
+12V
BAND B THRESHOLD
-5.2V
REDUCE SIGNAL
X
LOCK (TTL)
+5V
RESET
ATTEN. CONTROL
-12V
MAIN DAC END
CONVERTER ENABLE
MODULATION ENABLE
ERROR DAC STEP
ERROR DAC ENABLE
PRESET PARITY
CONVERTER SEQUENCER
(TO A105-J1) P2
(TO A204-J6) P3
(TO A204-J2) P4
(TO A204-J7) P5
(TO A204-J4) P6
E13 BAND B THRESHOLD
E14
E15 DETECTED MODULATION
E16 LOCK (ECL)
E17 ATTENUATOR CONTROL



5500090 - G

Figure 200-2. Converter Interconnect Schematic

A201
SOURCE AMPLIFIER
(2020091)

A source of up to one watt of power at 200 MHz is required to drive the step recovery diode Comb Generator in YIG Assembly A207. The 200 MHz must be both stable and coherent with the master oscillator in the counter. Stability is required to provide an IF spectrum that is dependent only upon the input signal spectrum. Coherence with the master oscillator is required to make counting accuracy dependent only upon the accuracy of the master oscillator.

The requirements of stability and coherence are satisfied by using a phase locked loop to lock a 200 MHz LC oscillator to the 10 MHz time base oscillator. The required output power is generated by a Class C amplifier that contains a leveling loop to set the power output at any desired level from 1 mW to 1.1 W.

CIRCUIT DESCRIPTION

The phase lock loop is a standard second order loop, implemented by using digital phase lock loop components. The 200 MHz LC oscillator is a modified Colpitts circuit with bias stabilization supplied by Q10. The output frequency of the 200 MHz oscillator is divided by 20 in U1 and U2 to produce a 10 MHz square wave. This signal is compared to the processed 10 MHz reference by phase detector U3. Phase error is amplified by active filter U4, and applied to voltage variable capacitor CR3. This holds the 200 MHz oscillator "locked" in phase to the 10 MHz reference signal. C23 sets the open loop center frequency of the oscillator.

The main power amplifier consists of four stages: buffer amplifier Q12 and Q13, linear amplifier Q14, and two Class C stages Q15 and Q16. Output power level is controlled by adjusting the value of the negative voltage supplied by Q17 and Q18 to the linear amplifier and Class C stages.

The power leveling loop operates by sampling the peak value of the output signal with CR5, and comparing this peak value to the Power Reference. The comparison is made by differential amplifier Q19 and Q20, which in turn controls Q17 and Q18.

PAGE LEFT BLANK INTENTIONALLY

A201 SOURCE AMPLIFIER

2020091-AB

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A201	Source Amplifier	2020091	1	EIP	34257
C1	Cer, .01μF, 20%, 100V	2150003	41	TG - S10	56289
C2	C1				
C3	Tant, 1.0μF, 10%, 35V	2300008	1	TAG20 - 1.0/35	14433
C4	Tant, 33μF, 10%, 10V	2300015	1	TAG20 - 33/10	14433
C5	Mica, 430pF, 5%, 500V	2250032	1	DM15-431J	72136
C6	Cer, .001μF, 20%, 1KV	2150001	6	5GA - D10	56289
C7 thru C10	C1				
C11	Cer, 20pF, NPO, 500V	2160016	2	301000C0G0200J	72982
C12	Cer, 18pF, NPO, 500V	2160007	1	301000C0G0180J	72982
C13	C1				
C14	Not Used				
C15	C1				
C16	Trim, 8-25pF, 250V	2350003	2	10S-T-22-8/25	0000X
C17	Cer, 4.7pF, NPO, 500V	2160013	2	301000C0H0479C	72982
C18	Cer, 15pF, NPO, 500V	2160006	2	301000C0H0150J	72982
C19	Cer, .01μF, 10%, 100V	2150014	1	5020EM100RD103K	EMCON
C20	Mica, 150pF, 5%, 500V	2250005	1	DM15 - 151J	72136
C21	C1				
C22	Cer, 12pF, NPO, 500V	2160005	3	301000C0G0120J	72982
C23	Trim, 2-8pF, 250V	2350001	1	10S-T-22-2/8	0000B
C24	Cer, 2.2pF, NPO, 500V	2160008	1	301000C0H0229J	72982
C25	Cer, 10pF, NPO, 500V	2160004	1	301000C0H0100C	72982
C26	C1				
C27	Tant, 47μF, 20%, 16V	2300025	1	TAG20 - 47/16-20	14433
C28	C1				
C29	C22				
C30	C22				
C31	C11				
C32	C1				
C33	C6				
C34	C6				
C35	C16				
C36	C17				
C37	C18				
C38	C1				
C39	Mica, 100pF, 5%, 500V	2250002	4	DM15 - 101J	72136
C40	Trim, 5.5-18pF, 250V	2350002	3	10S-T-22-5.5/18	0000X
C41	Cer, 24pF, NPO, 500V	2160010	4	301000C0G0240J	72982
C42	C41				
C43	C1				
C44	C1				

A201 SOURCE AMPLIFIER, continued 2020091 - AB

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C45	C40				
C46	C41				
C47 thru C49	C1				
C50	C39				
C51	C1				
C52	C40				
C53	C41				
C54	C1				
C55	C1				
C56	Trim, 5.5-18pF, 250V	2350022	1	10S-T-24-5.5/18	0000X
C57	C39				
C58	C39				
C59 thru C61	C1				
C62	Tant, 10μF, 20%, 25V	2300029	1	TAG20-10/25	14433
C63	C6				
C64 thru C66	C1				
C67	Mica, 33pF, 5%, 500V	2250014	1	DM15-330J	72136
C68	Not Used				
C69 thru C80	C1				
C81	C6				
C82	C6				
C83	C1				
C84	C1	2350028	1	CD6CD02D03	14655
C85	Mica, 2pF, 25%, 500V				
CR1	Hot Carrier	2710006	2	5082-2800	28480
CR2	General Purpose	2704154	8	IN4154	07263
CR3	Volt Var Cap	2710012	1	MV109	04713
CR4	CR2				
CR5	CR1				
CR6 thru CR11	CR2				
L1	Not Used				
L2	Not Used				
L3	100μH	3520007	1	1537-76	99800
L4	Jumper				
L5	Part of Board				

A201 SOURCE AMPLIFIER, continued 2020091-AB

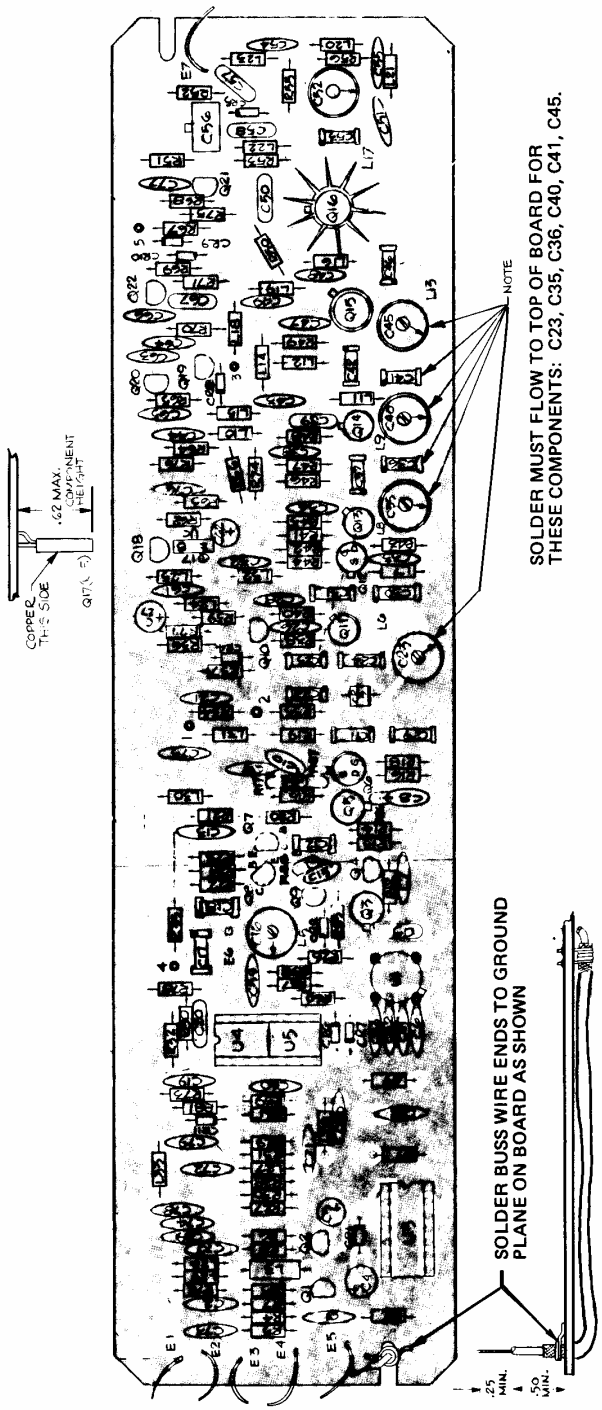
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
L6	Part of Board				
L7	1.0μH	3510003	4	DD-1.00	72259
L8	Part of Board				
L9	Part of Board				
L10	1.2μH	3510010	17	1025-22	99800
L11	0.1μH	3510001	1	DD-0.10	72259
L12	L7				
L13	Part of Board				
L14	L10				
L15	L10				
L16	L7				
L17	Part of Board				
L18 thru L21	L10				
L22	0.12μH	3510011	1	DD-0.12	72259
L23	L7				
L24 thru L33	L10				
Q1	NPN General Purpose	4704124	3	2N4124	04713
Q2	Q1				
Q3	PNP, RF Graded-Yellow	4710012	4	2N5179	
Q4	PNP, RF	4710010	2	MPS-H81	04713
Q5	Q3				
Q6	N-Chan, J-Fet	4704416	2	2N4416	04713
Q7	NPN, Silicon	4710026	2	NE73432B	04713
Q8	Q7				
Q9	Q4				
Q10	PNP, General Purpose	4704126	5	2N4126	04713
Q11	PNP, RF Graded-Green	4710013	1	2N5179	04713
Q12	Q6				
Q13	Q3				
Q14	Q3				
Q15	NPN, RF	4720002	2	2N3866	04713
Q16	Q15				
Q17	NPN, Power	4710003	1	MJE520	04713
Q18 thru Q21	Q10				
Q22	Q1				
R1	Comp, 2.2K, 5%, 1/4 W	4010222	1	RC07GF222J	81349
R2	Comp, 51, 2%, 1/4 W	4010510	1	C4/2%/51	24546
R3	Met Ox, 6.8K, 2%, 1/4 W	4130682	2	C4/2%/682	24546

A201 SOURCE AMPLIFIER, continued 2020091 - AB

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R4	Met Ox, 3.9K, 2%, 1/4 W	4130392	3	C4/2%/392	24546
R5	Met Ox, 270, 2%,1/4 W	4130271	1	C4/2%/271	24546
R6	Met Ox, 2K, 2%, 1/4 W	4130202	1	C4/2%/202	24546
R7	R4				
R8	R3				
R9	Met Ox, S.A.T.	4130999	3	S.A.T.	
R10	Not Used				
R11	Not Used				
R12	Comp, 390, 5%, 1/4 W	4010391	1	RC07GF391J	81349
R13	Comp, 110, 5%, 1/4 W	4010111	1	RC07GF111J	81349
R14	Met Ox, 240, 2%, 1/4 W	4130241	1	C4/2%/241	24546
R15	Comp, 820, 5%, 1/4 W	4010821	2	RC07GF821J	81349
R16	Comp, 1K, 5%, 1/4 W	4010102	2	RC07GF102J	81349
R17	Comp, 470, 5%, 1/4 W	4010471	1	RC07GF471J	81349
R18	Comp, 27K, 5%, 1/4 W	4010273	1	RC07GF273J	81349
R19	Met Ox, 5.6K, 2%, 1/4 W	4130562	1	C4/2%/562	24546
R20	Comp, 10K, 5%, 1/4 W	4010103	2	RC07GF103J	81349
R21	Comp, 1.6K, 5%, 1/4 W	4010162	1	RC07GF162J	81349
R22	Comp, 620, 5%, 1/4 W	4010621	1	RC07GF621J	81349
R23	Comp, 120, 5%, 1/4 W	4010121	1	RC07GF121J	81349
R24	R15				
R25	R16				
R26	Comp, 4.7K, 5%, 1/4 W	4010472	1	RC07GF472J	81349
R27	Met Ox, 510, 2%, 1/4 W	4130511	2	C4/2%/511	24546
R28	Met Ox, 220, 2%, 1/4 W	4130221	2	C4/2%/221	24546
R29	R27				
R30	Met Ox, 1.8K, 2%, 1/4 W	4130182	1	C4/2%/182	24546
R31	R28				
R32	Met Ox, 3.3K, 2%, 1/4 W	4130332	2	C4/2%/332	24546
R33	Met Ox, 24K, 2%, 1/4 W	4130243	3	C4/2%/243	24546
R34	Comp, 24K, 5%, 1/4 W	4010243	1	RC07GF243J	81349
R35	R33				
R36	Met Ox, 1K, 2%, 1/4 W	4130102	6	C4/2%/102	24546
R37	Met Ox, 11K, 2%, 1/4 W	4130113	2	C4/2%/113	24546
R38	Comp, 39K, 5%, 1/4 W	4010393	1	RC07GF393J	81349
R39	Met Ox, 200, 2%, 1/4 W	4130201	2	C4/2%/201	24546
R40	R36				
R41	Met Ox, 9.1K, 2%, 1/4 W	4130912	1	C4/2%/912	24546
R42	Met Ox, 3K, 2%, 1/4 W	4130302	2	C4/2%/302	24546
R43	Met Ox, 1.2K, 2%, 1/4 W	4130122	1	C4/2%/122	24546
R44	Met Ox, 820, 2%, 1/4 W	4130821	2	C4/2%/821	24546
R45	R36				
R46	R4				
R47	R42				
R48	R39				
R49	Met Ox, 30, 2%, 1/4 W	4130300	1	C4/2%/300	24546

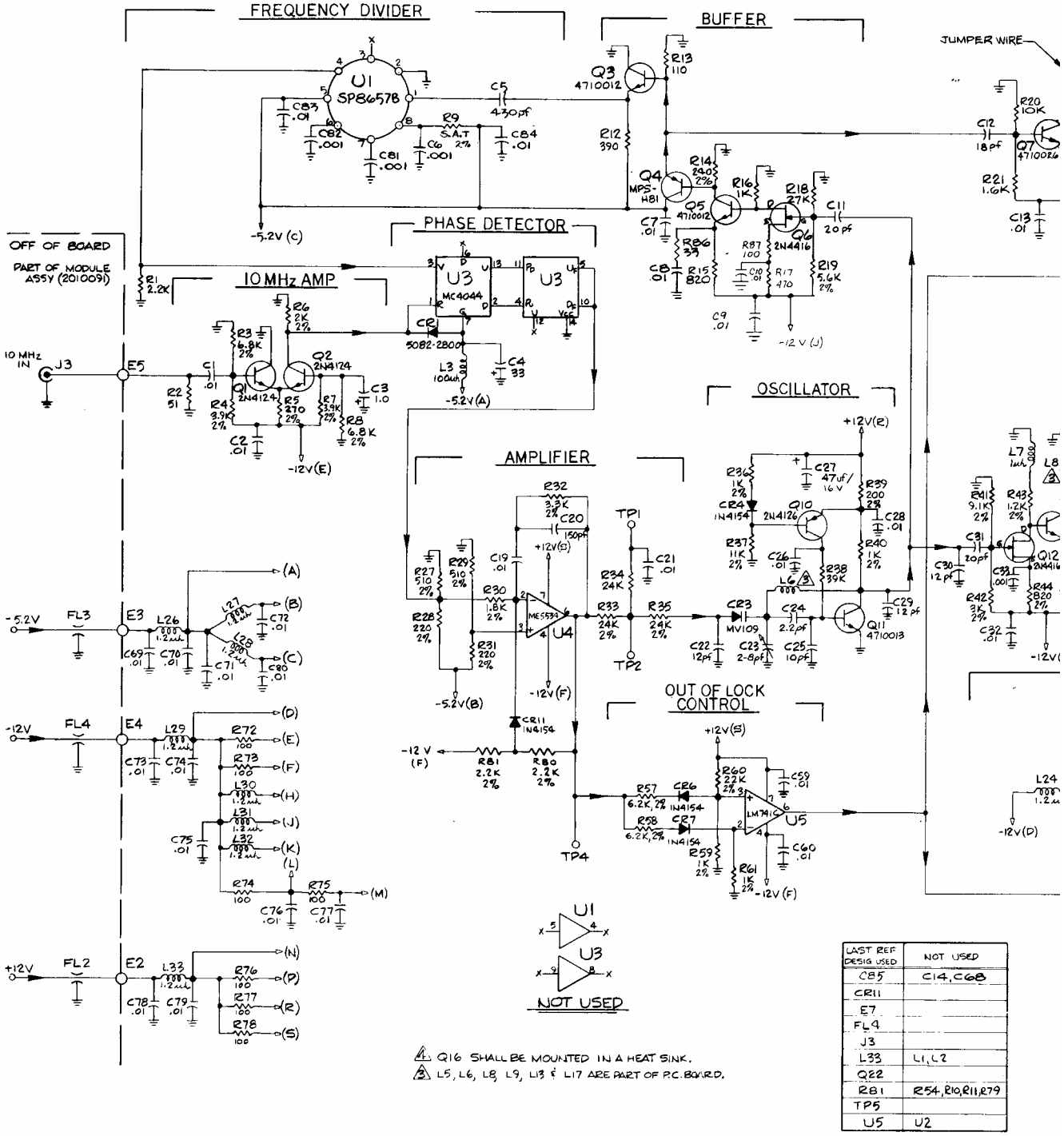
A201 SOURCE AMPLIFIER, continued - 2020091 - AB

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R50	R9				
R51	Met Ox, 6.2K, 2%, 1/4 W	4130622	3	C4/2%/622	24546
R52	R36				
R53	R33				
R54	Not Used				
R55	Met Ox, 1.1K, 2%, 1/4 W	4130112	1	C4/2%/1.1K	24546
R56	Met Ox, 100, 2%, 1/4 W	4130101	1	C4/2%/100	24546
R57	R51				
R58	R51				
R59	R36				
R60	Met Ox, 22K, 2%, 1/4 W	4130223	1	C4/2%/223	24546
R61	R36				
R62	Met Ox, 10K, 2%, 1/4 W	4130103	1	C4/2%/103	24546
R63	R37				
R64	R44				
R65	Met Ox, 2.7K, 2%, 1/4 W	4130272	1	C4/2%/272	24546
R66	Comp, 2.7K, 5%, 1/4 W	4010272	1	RC07GF272J	81349
R67	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/472	24546
R68	R9				
R69	R32				
R70	Comp, 100, 5%, 1/4 W	4010101	9	RC07GF101J	81349
R71	R20				
R72 thru R78	R70				
R79	Not Used				
R80	Met Ox, 2.2K, 2%, 1/4 W	4130222	2	C4/2%/222	24546
R81	R80				
R82 thru R85	Not Used				
R86	Comp, 33, 5%, 1/4 W	4010330	1	RC07GF330J	81349
R87	R70				
R88	Comp, 33 NOM	4010999	1	RC07GF S.A.T.	81349
U1	200 MHz, Hi-Speed ÷ 20	3010657	1	SP8657B	0000X
U2	Not Used				
U3	PHS/Frequency Detector	3014044	1	MC40441	04713
U4	Op Amplifier, Low Noise	3045534	1	NE5534N	72136
U5	Op Amplifier	3040741	1	741CN	0000X

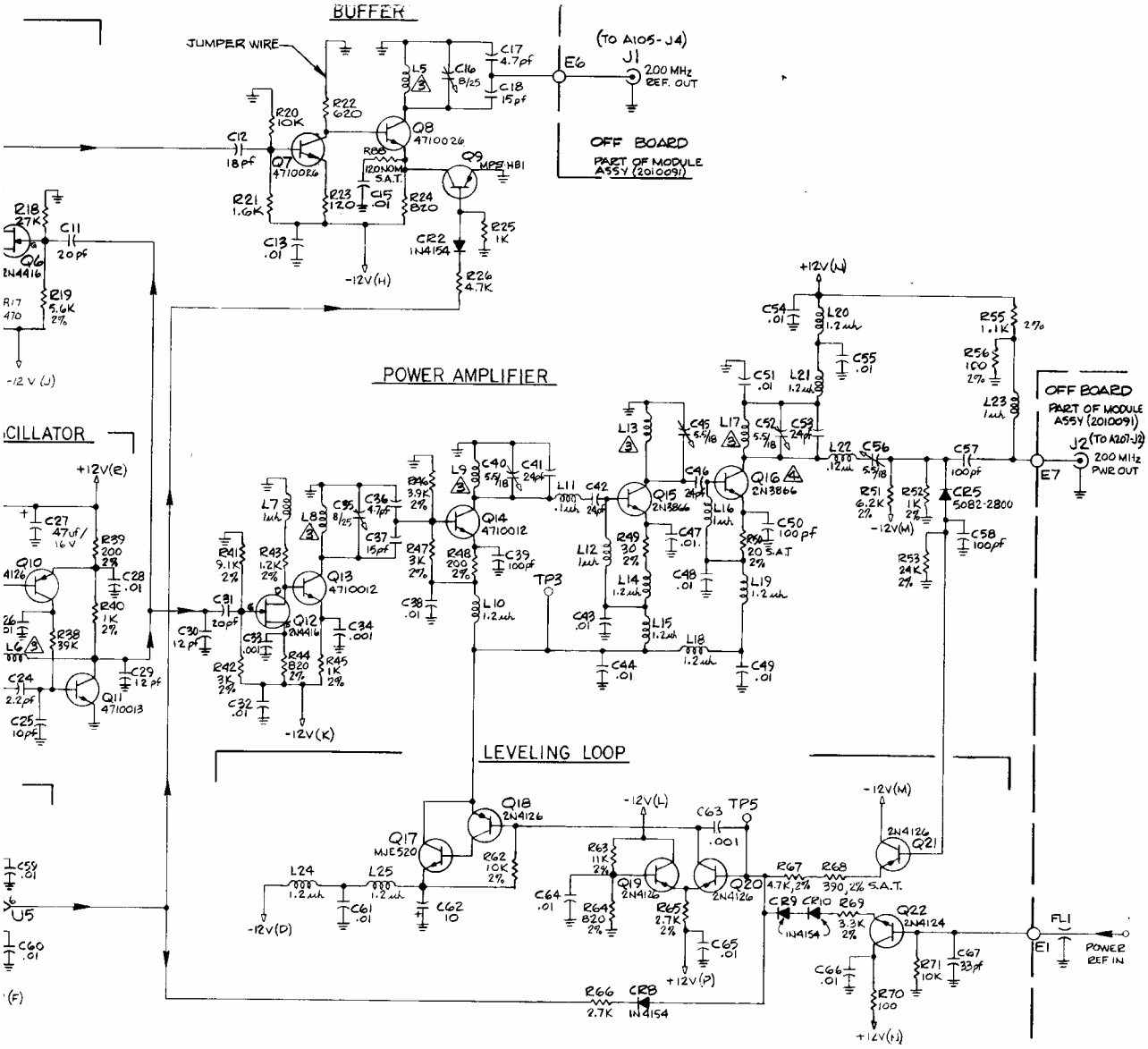


2020091 - AB

Figure 201-1. Source Amplifier Component Locator



LAST REF DESIG USED	NOT USED
C85	C14, C68
CR11	
E7	
FL9	
J3	
L33	L1, L2
Q22	
R81	R54, R10, R11, R79
TP5	
U5	U2



LAST REF DESIG USED	NOT USED
C85	C14, C68
CR11	
E7	
FL4	
J3	
L33	L1, L2
Q22	
RB1	R54, R10, R11, R79
TP5	
U5	U2

5500091 - R

Figure 201-2. Source Amplifier Schematic

A202
YIG CONTROL
(2020092)

The YIG Control Board (A202) contains circuits required to set the frequency of the YIG filter (A207) and to generate the BCD preset information for the Count Chain (A103). The main digital-to-analog converter (DAC) selects a particular comb line and provides the output frequency information. An error DAC provides a correction signal to precisely center the YIG filter passband on a comb line, based on information derived from the centering circuits. These circuits operate by modulating the center frequency of the YIG passband at a 20 kHz rate. This causes the filter to be tuned back and forth through the desired comb line, producing a pulse each time the YIG passes through the comb frequency. The phase of this detected modulation is then compared to the modulation frequency to produce the required centering information.

MAIN DAC

Steps of 200 MHz to the YIG filter are controlled by the main DAC. This DAC consists of a voltage reference (CR3, U12), presettable BCD counters (U19, U20), a series of transistor switches (Q3–Q10), precision summing resistors, and a summing amplifier (U13). Data from the front panel thumbwheel switch is preset into U19 and U20 during the Reset period. Each output line controls a transistor switch which connects a precision resistor to the 3.1V voltage reference. The value of the resistor determines the current into the SUM line, while the summing amplifier provides a voltage output proportional to the total input current. The digital output of U19 and U20 are also used to provide 3MSD preset information to A103.

In the AUTO mode, pulses from A203 into the clock input of U19 cause the DAC to step in 200 MHz increments upon command. In the MANUAL mode, a Parity Checker (U16, U17, U18), compares the thumbwheel information with the actual states of U19 and U20. If they differ, an output is obtained which triggers a Reset, and in turn causes the DAC output to equal the thumbwheel switch setting.

YIG DRIVER

The voltage output of the summing amplifier is converted into a current in the YIG Driver (U14, Q11, Q12, and chassis mounted A2Q1). R89 sets the current offset, while R87 sets the slope. The current sense resistor (R92) provides the required feedback voltage for the driver. CR5 limits the voltage across the YIG filter tuning coil during Reset in order to protect Q12 and A2Q1.

YIG PASSBAND MODULATION

As part of the centering function, the center frequency of the YIG passband is modulated by means of an auxiliary tuning coil within the YIG. A 40 kHz clock is divided in U4 to produce a 20 kHz square wave. This signal is converted to a triangular waveform by integrator U11. This output is then converted to a current in the Modulation Coil Driver. Q14–Q16 form a high gain voltage amplifier. The single ended output at the collector of Q16 is converted to a bipolar output with Q17 and Q19, while CR7 and CR8 compensate for base emitter junction voltages. Q18 and Q20 provide increased current capability. Feedback for the driver is supplied by sensing the current through R107, thus converting the voltage input to a current output. Nominal deviation of the YIG center frequency is ± 50 MHz.

YIG CENTERING CIRCUIT

Centering of the YIG passband is achieved by detecting the output of the modulated comb generator and phase comparing it to the modulation frequency in U1. U1 is a four quadrant multiplier, producing outputs proportional to the product of two inputs. The positive and negative outputs of U1 differentially drive an active low pass filter (U2), which in turn, drives another low pass filter (U3). The output of U3 represents the DC component of the output of U1. Its amplitude and sign are directly related to the frequency offset of the YIG filter passband from the comb frequency. This signal is sensed by window detector U5. If the output at U3 exceeds the threshold reference, one of the two outputs of U5 is driven high.

The two outputs of U5 are used to control the Error DAC. This DAC supplies an error signal directly into the Main DAC summing amplifier. R42-R48 are summing resistors switched on by U9 and U10 (binary up-down counters). Clock pulses from U4 at a 2.5 kHz rate cause U9 to either count up, count down, or remain fixed depending on the outputs of U5.

Thus, a continually increasing (or decreasing) error signal is applied to the main tuning coil of the YIG until the DC output of U3 falls inside the threshold limits. The Borrow output of U10 provides a low level clamp on the DAC, while the C output of U10 provides a high level clamp. The Error DAC step at U6 pin 11 provides the information to the Converter Sequencer (A203) that the YIG centering cycle is completed.

A202 YIG CONTROL

2020092 - V

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A202	YIG Control	2020092	1	EIP	34257
C1	Cer, .05μF, 20%, 20V	2150010	2	UK20-503	71590
C2	C1				
C3	Cer, .01μF, 20%, 100V	2150003	20	TG - S10	56289
C4 thru C6	C3				
C7	Cer, .005μF, 20%, 100V	2150008	2	TG - D50	56289
C8	Cer, .001μF, 20%, 1KV	2150001	3	5GA - D10	56289
C9 thru C11	C3				
C12	Mica, 1000pF, 5%, 500V	2250003	1	DM15 - 102J	72136
C13	Cer, .02μF, 20%, 100V	2150006	1	TG - S20	56289
C14	Tant, 10μF, 25V	2300029	3	TAG20 - 10/25	14433
C15	C3				
C16	C3				
C17	C7				
C18	C3				
C19	C8				
C20	Tant, 0.1μF, 35V	2300020	1	TAG20 - 0.1/35	14433
C21	C3				
C22	Tant, 1μF, 35V	2300008	1	TAG20 - 1.0/35	14433
C23	C8				
C24	Mica, 180pF, 5%, 500V	2250006	1	CM15-181J	72136
C25	Mica, 33pF, 5%, 500V	2250014	2	DM15-330J	72136
C26	C25				
C27	C14				
C28	C14				
C29	Tant, 33μF, 20V	2300023	2	TAG20 - 33/20	14433
C30 thru C32	C3				
C33	Tant, 33μF, 10V	2300015	2	TAG20 -33/10	14433
C34	C3				
C35	C33				
C36 thru C39	C3				
C40	C29				
C41	C3				
CR1	Zener, 5.1V	2705231	1	IN5231	04713
CR2	General Purpose	2704154	4	IN4154	04713
CR3	Zener, 6.2V	2700827	1	IN827	04713

A202 YIG CONTROL, continued - 2020092 - V

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
CR4	CR2				
CR5	Zener, 51V	2704757	1	IN4757	04713
CR6	Rectifier	2704001	1	IN4001	04713
CR7	CR2				
CR8	CR2				
Q1	NPN, General Purpose	4704124	5	2N4124	04713
Q2	N-Channel, J FET	4710022	1	T1S73	01295
Q3	NPN	4704401	8	2N4401	04713
Q4 thru Q10	Q3				
Q11	Q1				
Q12	PNP, Amplifier	4710018	1	MPS - L51	04713
Q13	Not Used				
Q14	Q1				
Q15	Q1				
Q16	PNP, General Purpose	4704126	3	2N4126	04713
Q17	Q1				
Q18	PNP	4710009	1	MJE - 350	04713
Q19	Q16				
Q20	NPN, Power	4710003	1	MJE - 520	04713
Q21	Q16				
R1	Met Ox, 10K,2%, 1/4 W	4130103	6	C4/2%/10K	24546
R2	R1				
R3	Met Ox, 2.2K, 2%, 1/4 W	4130222	3	C4/2%/2.2K	24546
R4	R3				
R5	Met Ox, 3.0K, 2%, 1/4 W	4130302	2	C4/2%/3K	24546
R6	Met Ox, 7.5K, 2%, 1/4 W	4130752	2	C4/2/7.5K	24546
R7	Met Ox, 11K, 2%, 1/4 W	4130113	4	C4/2%/11K	24546
R8	R7				
R9	R5				
R10	R3				
R11	Met Ox, 2K, 2%, 1/4 W	4130202	1	C4/2%/2K	24546
R12 thru R15	R1				
R16	Met Ox, 20K, 2%, 1/4 W	4130203	2	C4/2%/20K	24546
R17	R16				
R18	Comp, 6.8K, 5%, 1/4 W	4010682	1	RC07GF682J	81349
R19	Comp, 13K, 5%, 1/4 W	4010133	1	RC07GF133J	81349
R20	Comp, 51K, 5%, 1/4 W	4010513	1	RC07GF513J	81349
R21	Comp, 1.1K, 5%, 1/4 W	4010112	1	RC07GF112J	81349
R22	Comp, 100, 5%, 1/4 W	4010101	2	RC07GF101J	81349
R23	Comp, 2.4K, 5%, 1/4 W	4010242	2	RC07GF242J	81349

A202 YIG CONTROL, continued 2020092 - V

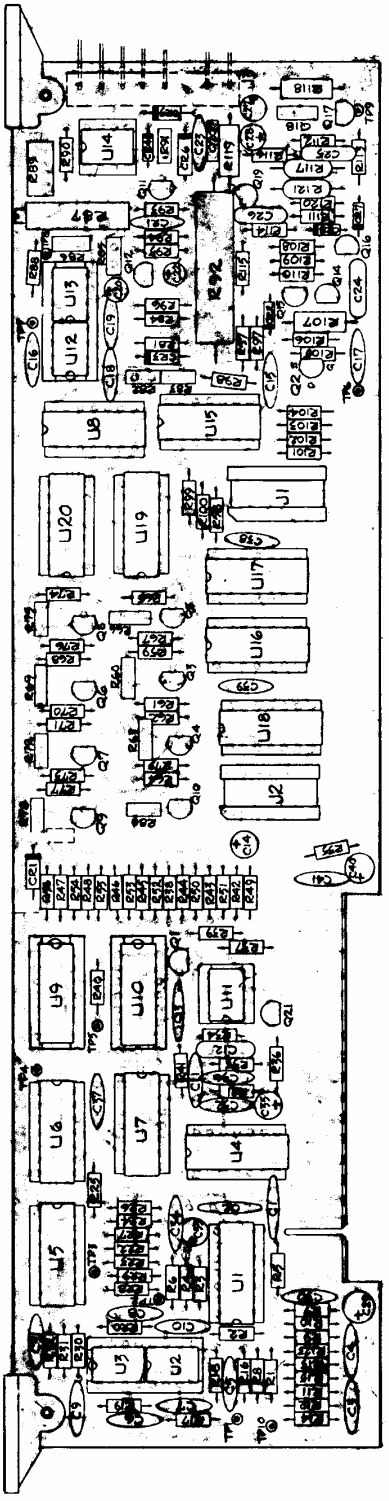
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R24	Comp, 910, 5%, 1/4 W	4010911	2	RC07GF911J	81349
R25	Comp, 2.2K, 5%, 1/4 W	4010222	13	RC07GF222J	81349
R26	Comp, 47K, 5%, 1/4 W	4010473	2	RC07GF473J	81349
R27	Comp, 1K, 5%, 1/4 W	4010102	4	RC07GF102J	81349
R28	R27				
R29	R26				
R30	R24				
R31	R23				
R32	R22				
R33	Comp, 10K, 5%, 1/4 W	4010103	6	RC07GF103J	81349
R34	Comp, 100K, 5%, 1/4 W	4010104	2	RC07GF104J	81349
R35	R6				
R36	R33				
R37	R34				
R38	R25				
R39	R27				
R40	R25				
R41	Comp, 200, 5%, 1/4 W	4010201	1	RC07GF201J	81349
R42	Cmt Film, 1M, 1%,	4120010	1	CC1004F	01121
R43	Cmt Film, 2M, 1%	4120011	1	CC2004F	01121
R44	Cmt Film, 4.02M, 1%	4120012	1	CC4024F	01121
R45	Comp, 8.2M, 5%, 1/4 W	4010825	1	RC07GF825J	81349
R46	Comp, 16M, 5%, 1/4 W	4010166	1	RC07GF166J	81349
R47	Comp, 33M, 5%, 1/4 W	4010336	1	RC07GF336J	81349
R48	Comp, 62M, 5%, 1/4 W	4010626	1	RC07GF626J	81349
R49	Comp, 2.7K, 5%, 1/4 W	4010272	14	RC07GF272J	81349
R50 thru R55	R49				
R56	Comp, 270, 5%, 1/4 W	4010271	1	RC07GF271J	81349
R57	Comp, 5.1K, 5%, 1/4 W	4010512	1	RC07GF512J	81349
R58	R25				
R59	R49				
R60	Prec, 400K, 0.5%, 1/2 A	4104003	1	AME55-C1-4003D	14298
R61	R33				
R62	R49				
R63	Prec, 200K, .25%, 1/2 W	4102003	1	AME55-C3-2003D	14298
R64	R33				
R65	R49				
R66	Prec, 100K, 0.1%, 1/2 W	4101003	1	AME55-C3-1003D	14298
R67	R33				
R68	R49				
R69	Prec, 80K, 0.1%, 1/2 A	4108002	1	AME55-C3-8002D	14298
R70	R33				
R71	R49				
R72	Prec, 40K, .05%	4140033	1	4S8P1S8	05591

A202 YIG CONTROL, continued 2020092 - V

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R73	Comp, 12K, 5%, 1/4 W	4010123	1	RC07GF123J	81349
R74	R49				
R75	Prec, 20K, .025%,	4140032	1	4S8P1S8	05591
R76	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R77	R49				
R78	Prec, 10K, .01%,	4140031	1	4S8P1S8	05591
R79	R25				
R80	Prec, 8K, .01%	4140030	1	4S8P1S8	05591
R81	Prec, 750, 1%, 1/10 W	4057500	1	RN55C750F	81349
R82	Prec, 8K, .1%,	4140035	2	4S8P1S8	05591
R83	R82				
R84	Comp, 1.5K, 5%,1/4 W	4010152	1	RC07GF152J	81349
R85	Prec, 3.0K, .1%	4140034	2	4S8P1S8	05591
R86	Prec, 3.7K, .1%	4140039	1	4S8P1S8	05591
R87	Variable, 500	4280009	1	89PR500	73138
R88	Prec, 12.1K, 1%, 1/10 W	4051212	1	RN55C1212F	81349
R89	Variable, 1K	4250003	1	72XWR1K	73138
R90	Prec, 39.2K, 1%	4053922	1	RN55C3922F	81349
R91	R85				
R92	WW, 5, 1%, 7W	4110003	1	T7(10PPM)	12436
R93	Comp, 1.6K, 5%, 1/4 W	4010162	1	RC07GF162J	81349
R94	Comp, 390, 5%, 1/4 W	4010391	2	RC07GF391J	81349
R95	R94				
R96	R27				
R97 thru R104	R25				
R105	Comp, 6.8K N.O.M.	4010999	1	RC07GFS.A.T.	81349
R106	Comp, 15K, 5%, 1/4 W	4010153	2	RC07GF153J	81349
R107	Comp, 10, 5%, 1/2 W	4020100	3	RC07GF100J	81349
R108	Comp, 4.3K, 5%, 1/4 W	4010432	1	RC07GF432J	81349
R109	Comp, 510, 5%, 1/4 W	4010511	1	RC07GF511J	81349
R110	R106				
R111	Comp, 3.9K, 5%, 1/4 W	4010392	1	RC07GF393J	81349
R112	R7				
R113	Met Ox, 180, 2%, 1/4 W	4130181	2	C4/2%/180	24546
R114	R113				
R115	R7				
R116	Comp, 120, 5%, 1/4 W	4010121	2	RC07GF121J	81349
R117	WW, 30, 5%, 1 W	4110010	2	239E3005	56289
R118	R107				
R119	R107				
R120	R116				
R121	R117				
R122	Not Used				
R123	Met Ox, 200 NOM	4130999	1	C4/2%/200 SAT	24546

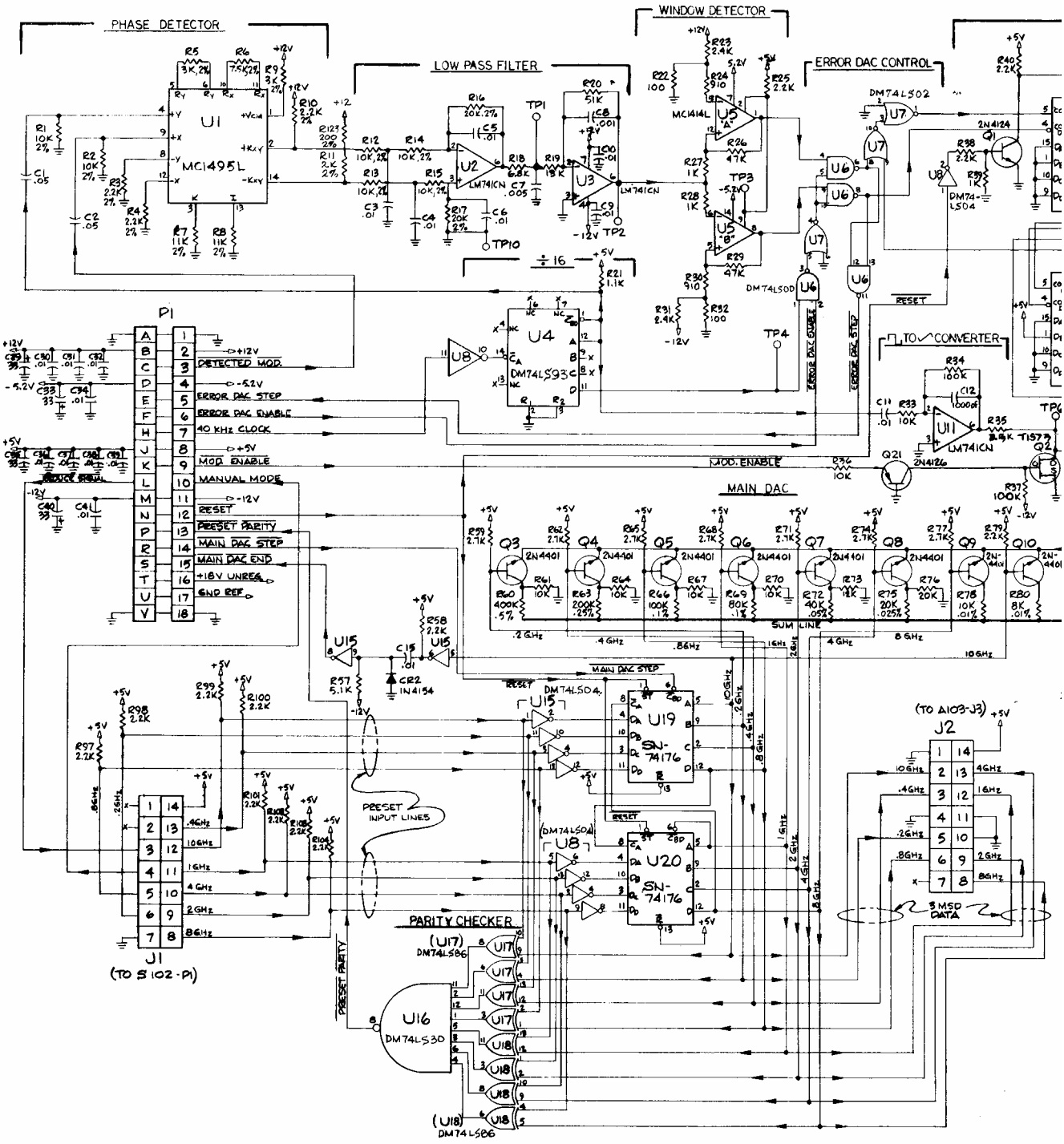
A202 YIG CONTROL, continued 2020092 - V

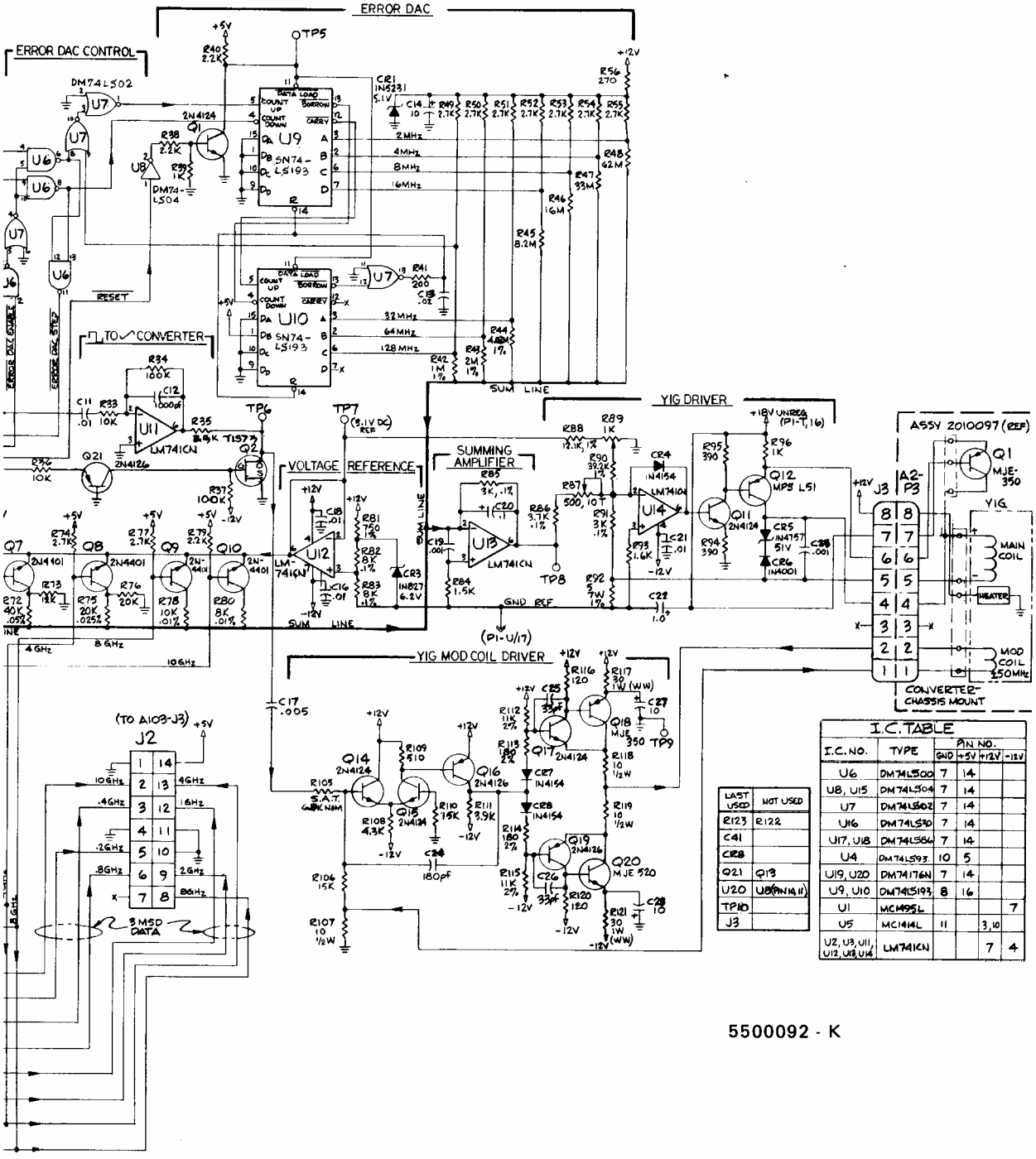
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U1	4-Quad Multiplier	3011495	1	MC1495L	04713
U2	Op Amplifier	3040741	6	LM741CN	27014
U3	U2				
U4	4-Bit Binary Counter	3087493	1	DM74LS93	27014
U5	Dual Diff. Comp	3011414	1	MC1414L	04713
U6	Quad NAND Gate	3087400	1	DM74LS00	27014
U7	Quad, 2 INP NOR Gate	3087402	1	DM74LS02	27014
U8	Hex Inverter	3087404	2	DM74LS04	27014
U9	UP/Down Binary Counter	3084193	2	SN74LS193	01295
U10	U9				
U11 thru U14	U2				
U15	U8				
U16	8 INP NAND Gate	3087430	1	DM74LS30	27014
U17	Quad 2 INP Ex Or Gate	3087486	2	DM74LS86	27014
U18	U17				
U19	Preset Decade Counter	3074176	2	SN74176N	01295
U20	U19				



2020092 - V

Figure 202-1. YIG Control Component Locator


PHASE DETECTOR
LOW PASS FILTER
WINDOW DETECTOR
ERROR DAC CONTROL
MC1495L
LM741CN
DM74LS93C
DM74LS02
DM74LS04
DM74LS86
DM74LS30
SN-74176
2N4401
2N4126
2N4124
MAIN DAC
SUM LINE
PRESET INPUT LINES
PARITY CHECKER
MOD ENABLE
RESET
MAIN DAC STEP
ERROR DAC STEP
ERROR DAC ENABLE
40 kHz CLOCK
MANUAL MODE
PRESET PARITY
MAIN DAC END
+18V UNREG
GND REF
DETECTED MOD.
TO ∿ CONVERTER
(TO A103-J3)
(TO S102-P1)
8 MSD DATA



5500092 - K

Figure 202-2. YIG Control Schematic

A203
CONVERTER SEQUENCER
(2020093)

The Converter Sequencer (A203) generates the signals required to step the RF Converter (A2) through its specified frequencies. The board contains a Sequence Generator to generate properly timed start and stop commands for all the required functions. Among the circuits controlled are: the attenuator control and driver circuitry for leveling and switching of the incoming signal, the power level control circuit for controlling the YIG comb power, and Error DAC (digital-to-analog converter) signals controlling the timing of the YIG filter centering circuitry.

SEQUENCE GENERATOR

The basic part of the Converter Sequencer is the Sequence Generator, composed of a binary counter (U8) and a de-multiplexer (U10). This circuit generates eight discrete steps, each of which is identified by a low on a corresponding test point (TP0-TP7).

U8 is driven by a 40 kHz clock (U18) through a network of gates which allow holding the Sequence Generator in any given step until a set of specific conditions signifies that the step is completed. The function of each sequence is shown in Figure 203-1.

Sequence 0 is the state the converter sequence goes to when the conveter is disabled. Sequence 0 sets a latch (U12 pin 1) whose output turns off the RF signal by setting the attenuator driver to maximum attenuation, and sending a command to the YIG Control board (A202) to begin the 20 kHz YIG coil modulation. Sequence 0 also sends out a Main DAC step command which steps the Main DAC to the next comb line unless the Converter is being disabled. If so, the disable reset command over-rides the DAC step, and the YIG stops at the bottom (or preset) frequency.

Sequence 1 begins the YIG power leveling cycle. A 1.5 ms one-shot (U11) resets the YIG power DAC (U19) for minimum power, and sets a latch (U15 pins 3, 8), whose output inhibits the clock into the Sequence Generator until the power leveling cycle is complete. At the end of the 1.5 ms reset time, the YIG power DAC begins increasing the LO power into the Mixer until the detected modulation (P1 pin 3) exceeds its threshold, or the LO power reaches its maximum output. At this point the U15 latch is reset which stops the clocking of the power DAC and allows the Sequence Generator to move to the next step.

Sequence 2 begins the YIG coil centering cycle. The centering circuitry is located on the YIG Control board (A202), but the enable time is controlled by the Converter Sequencer.

A 1 ms one-shot is triggered by Sequence 2. Two outputs are taken from the one-shot: the Q output which is used as an Error DAC enable signal to turn on the centering circuitry on the YIG Control board; and $\overline{Q}$ output which is fed back to hold the Sequence Generator in Sequence 3 until the centering process is completed. The end of this process is indicated by a lack of error DAC step pulses. When this occurs, the one-shot times out, and the Sequence Generator is released to go on to Sequence 4.

Sequence 4 is the first step of the sequence in which the input signal is examined. In this step, the latch (U12 pin 1) controlling the input signal is reset; this also turns off the YIG modulation. A second latch (U12 pin 12) is set at the start of Sequence 4. This latch inhibits the sequence during Sequence 5 until a Band B Threshold signal is obtained. This step thus guarantees that at least one input signal has been received during either Sequence 4 or 5.

Sequence 6 is used as a 25 μ sec delay period to provide the necessary time for operation of the Attenuator Control on signals with slow rise times. This is discussed further in the Attenuator Control paragraphs below.

Sequence 7 is the LOCK sensing portion of this sequence. If the signal received during Sequence 4 or 5 results in a LOCK command from the IF Processor, then the sequence will remain in Sequence 7, and send a LOCK command to the Control board (A104) in the Basic Counter. If no LOCK was obtained, the Sequencer will continue to Sequence 0, and repeat the sequence with the next comb line.

ATTENUATOR CONTROL

The Attenuator Control circuits perform the function of limiting the variations in input signal amplitude as seen by the Mixer (A205). The ATTENUATOR CONTROL command from the IF Processor (A204) is activated whenever the input signal received by A205 exceeds the minimum signal by at least 7 dB. This command triggers one-shot U3. The output of U3 drives a DAC consisting of a counter (U4), summing resistors (R9-R14), a summing amplifier (U5), and an inverting amplifier (U6). Each DAC step results in a nominal 0.5 dB increase in attenuator insertion loss. The REDUCE SIGNAL indicator on the front panel is activated when the DAC reaches its 32nd step.

The DAC acts as a sample and hold circuit for attenuation level. As long as there is insufficient attenuation, the ATTENUATOR CONTROL command will cause the attenuation to increase 0.5 dB for each input pulse. On long pulses or CW signals, U3 will retrigger as long as the ATTENUATOR CONTROL command remains active.

In addition to increasing attenuator insertion loss, the ATTENUATOR CONTROL command forces the Sequence Generator to Sequence 3 by activating the preset strobe line of U8. Since the RF switch remains open, and the YIG modulation is not enabled, the Sequencer then moves on through Sequence 4 and 5, and again waits for Band B Threshold. The result is that the Sequencer cannot go on to Sequence 6 until the attenuator has reduced the input signal sufficiently.

ATTENUATOR DRIVER

The output of U6 is a voltage corresponding to the desired attenuation. This signal is converted into two related currents by the Attenuator Driver. These currents: I_{total} and I_{series}, determine both the attenuation and the input VSWR of the PIN Diode Attenuator (part of A206).

Series current is generated by the network of U5 and Q6. R53 is the sense resistor for the current source. The non-linear current output versus input level is achieved with a double breakpoint shaping network — Q2 and Q3 form one breakpoint, while Q4 and Q5 form the other. Variable resistor R47 sets the series current, and optimizes VSWR, at high attenuation levels.

Total current is the sum of series current and shunt current. The shunt current waveform is shaped by diode network CR2, CR3, and their associated resistors. Variable resistor R23 is used to adjust the ratio between series and shunt currents at moderate attenuation levels. U6 and current booster Q1, combine series and shunt networks to produce the total current output.

POWER LEVEL CONTROL

During Sequence 1, the YIG comb level is set. This function is accomplished by varying the POWER REFERENCE level into the Source/Amplifier (A201). This in turn varies the 200 MHz power into the YIG/Comb Generator (A207). The comb line output is detected by the Mixer, and sensed by the Threshold Detector U17. Variable resistor R64 sets the threshold level.

Operation of the Power Level Control begins at the end of the 1.5 ms period of U11. Clock pulses from U18 are then allowed to step the Power Level DAC (U19, R74 thru R80). When the comb output exceeds the threshold, U17 triggers, resetting the latch (U15 pin 10), inhibiting the clock input to the DAC and ending the sequence. If the DAC reaches maximum output, the same result is obtained.

SEQUENCE	FUNCTIONS	DURATION
0	1. Attenuator to max attenuation. 2. YIG Modulation enabled. 3. Main DAC step. 4. Reset state.	25 μ s unless held by RESET.
1	1. YIG comb leveling cycle.	1.5 - 4.7 msec.
2	1. Initiate YIG centering cycle.	25 μ seconds.
3	1. YIG centering cycle.	1 - 10 mseconds.
4	1. Attenuator to normal control. 2. Modulation off. 3. Initiate wait for Band B Threshold.	25 μ seconds.
5	1. Wait for Band B Threshold.	Depends upon PRF.
6	1. 25 μ second delay.	25 μ seconds.
7	1. LOCK sensing sequence.	25 μ sec if no LOCK.

FIGURE 203-1. CONVERTER SEQUENCE FUNCTIONS

A203 CONVERTER SEQUENCER

2020093 - DE

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A203	Converter Sequencer	2020093	1	EIP	34257
C1	Cer, .01μF, 20%, 100V	2150003	17	TG - S10	56289
C2	C1				
C3	C1				
C4	Cer, .005μF, 20%, 100V	2150008	1	TG - S10	56289
C5	C1				
C6	C1				
C7	Tant, .47μF, 35V	2300005	2	TAG20 - .47/35	14433
C8	C1				
C9	C1				
C10	Tant, 10μF, 25V	2300029	3	TAG20 - 10/25	14433
C11	Tant, 1.0μF, 35V	2300008	1	TAG20 - 1.0/35	14433
C12	Tant, 33μF, 20%, 10V	2300015	4	TAG20 - 33/10	14433
C13	C1				
C14	C1				
C15	Mica, 33pF, 5%, 500V	2250014	1	DM15 - 330J	72136
C16	C7				
C17	C1				
C18	C12				
C19	Mica, 1000pF, 5%, 500V	2250003	DM15 -	102J	72136
C20 thru C22	C1				
C23	C10				
C24	C1				
C25	C12				
C26	C1				
C27	C1				
C28	C12				
C29	C1				
C30	C10				
C31	Tant, .39μF, 10%, 35V	2300026	1	196D394X9035HA1	56289
CR1	General Purpose	2704154	4	IN4154	07263
CR2	CR1				
CR3	Hot Carrier	2710004	1	FH1100	07263
CR4	Zener, 4.7V	2705230	2	IN5230	04713
CR5	Zener, 8.2V	2705237	1	IN5237	04713
CR6	Rectifier	2704001	1	IN4001	04713
CR7	CR				
CR8	Zener, 3.6V	2705227	1	IN5227	04713
CR9	Zener, 5.1V	2705231	1	IN5231	04713
CR10	CR4				

A203 CONVERTER SEQUENCER, continued

2020093 - DE

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
Q1	NPN, General Purpose	4704124	3	2N4124	04713
Q2	Q1				
Q3	PNP, General Purpose	4704126	3	2N4126	04713
Q4	Q1				
Q5	Q3				
Q6	Q3				
R1	Comp, 200, 5%, 1/4 W	4010201	1	RC07GF200J	81349
R2	Comp, 12K, 5%, 1/4 W	4010123	1	RC07GF123J	81349
R3	Comp, 5.1K, 5%, 1/4 W	4010512	8	RC07GF512J	81349
R4 thru R6	R3				
R7	Comp, 1K, 5%, 1/4 W	4010102	3	RC07GF102J	81349
R8	Comp, 1.5K, 5%, 1/4 W	4010152	2	RC07GF152J	81349
R9	Comp, 620K, 5%, 1/4 W	4010624	2	RC07GF624J	81349
R10	Comp, 330K, 5%, 1/4 W	4010334	2	RC07GF334J	81349
R11	Comp, 160K, 5%, 1/4 W	4010164	2	RC07GF164J	81349
R12	Comp, 75K, 5%, 1/4 W	4010753	2	RC07GF753J	81349
R13	Comp, 39K, 5%, 1/4 W	4010393	1	RC07GF393J	81349
R14	Met Ox, 18K, 2%, 1/4 W	4130183	3	C4/2%/18K	24546
R15	R8				
R16	Comp, 8.2K, 5%, 1/4 W	4010822	3	RC07GF822J	81349
R17	Met Ox, 27K NOM, S.A.T.	4130999	4	C4/2%/S.A.T.	24546
R18	Comp, 430K, NOM, S.A.T.	4010999	3	RC07GFSAT	81349
R19	Met Ox, 10K, 2%, 1/4 W	4130103	3	C4/2%/10K	24546
R20	R7				
R21	Variable, 10K	4250006	2	72XWR10K	73138
R22	Comp, 5.6, 5%, 1/4 W	4010569	2	RC07GF569J	81349
R23	Met Ox, 1.2K, 2%, 1/4 W	4130122	2	C4/2%/1.2K	24546
R24	Met Ox, 1.5K, 2%, 1/4 W	4130152	2	C4/2%/1.5K	24546
R25	S.A.T.				
R26	Comp, 470, 5%, 1/4 W	4010471	6	RC07GF471J	81349
R27	Comp, 82, 5%, 1 W	4030820	1	RC32GF820J	81349
R28	Comp, 10K, 5%, 1/4 W	4010103	1	RC07GF103J	81349
R29	R19				
R30	Met Ox, 2.2K, 2%, 1/4 W	4130222	1	C4/2%/222	24546
R31	R19				
R32	R16				
R33	Comp, 100, 5%, 1/4 W	4010101	1	RC07GF101J	81349
R34	Comp, 16K, 5%, 1/4 W	4010163	2	RC07GF163J	81349
R35	R22				
R36	R16				
R37	Comp, 47K, 5%, 1/4 W	4010473	1	RC07GF473J	81349
R38	R34				
R39	Met Ox, 15K, 2%, 1/4 W	4130153	1	C4/2%/153	24546
R40	R23				

A203 CONVERTER SEQUENCER, continued

2020093 - DE

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R41	Met Ox, 1K, 2%, 1/4 W	4130102	1	C4/2%/102	24546
R42	Prec, 8.66K, 1%, 1/8 W	4068661	2	RN55D8661F	81349
R43	R42				
R44	Variable, 1K	4250003	1	72XWR1K	73138
R45	Met Ox, 430, 2%, 1/4 W	4130431	1	C4/2%/413	24546
R46	Met Ox, 270, 2%, 1/4 W	4130271	1	C4/2%/271	24546
R47	Met Ox, 1.8K, 2%, 1/4 W	4130182	4	C4/2%/182	24546
R48	R26				
R49	Comp, 2K, 5%, 1/4 W	4010202	1	RC07GF202J	81349
R50	Met Ox, 24, 2%, 1/4 W	4130240	1	C4/2%/240	24546
R51	Comp, 39, 5%, 1/4 W	4010390	1	RC07GF390J	81349
R52	R47				
R53	Met Ox, 20K, 2%, 1/4 W	4130203	1	C4/2%/203	24546
R54	Met Ox, 24K, 2%, 1/4 W	4130243	1	C4/2%/243	24546
R55	Comp, 4.7K, 5%, 1/4 W	4010472	3	RC07GF472J	81349
R56	Comp, 5.6K, 5%, 1/4 W	4010562	1	RC07GF562J	81349
R57	R55				
R58	Comp, 6.2K, 5%, 1/4 W	4010622	1	RC07GF622J	81349
R59	R26				
R60	R26				
R61	R7				
R62	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R63	R26				
R64	Comp, 2.4K, 5%, 1/4 W	4010242	1	RC07GF242J	81349
R65	Comp, 33K, 5%, 1/4 W	4010333	2	RC07GF333J	81249
R66	R55				
R67	R47				
R68	R47				
R69	Comp, 3.9K, 5%, 1/4 W	4010392	1	RC07GF392J	81349
R70 thru R73	R3				
R74	Met Ox, 8.2K, 2%, 1/4 W	4130822	1	C4/2%/822	24546
R75	R14				
R76	Comp, 36K, 5%, 1/4 W	4010363	1	RC07GF363J	81349
R77	R12				
R78	R11				
R79	R10				
R80	R9				
R81	R18				
R82	Comp, 220, 5%, 1/4 W	4010221	1	RC07GF221J	81349
R83	R14				
R84	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/392	24546
R85	R17				
R86	R17				
R87	Met Ox, 2.0K, 2%, 1/4 W	4130202	1	C4/2%/202	24546

A203 CONVERTER SEQUENCER, continued

2020093 - DE

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R88	Comp, 3.6K, 5%, 1/4 W	4010362	1	RC07GF362J	81349
R89	Comp, 180, 5%, 1/4 W	4010181	1	RC07GF181J	81349
R90	R21				
R91	Comp, 3K, 5%, 1/4 W	4010302	1	RC07GF302J	81349
R92	R65				
R93	R17				
R94	R24				
R95	R26				
R96	Comp, 750, 5%, 1/4 W	4010751	1	RC07GF751J	81349
U1	Quad Translator	3110125	1	MC10125L	0000X
U2	2 INP NOR Gate	3087402	1	DM74LS02	01295
U3	Mulitvibrator	3084123	1	DM74LS123	01295
U4	4 bit Binary Counter	3084393-02	2	DM74LS393	01295
U5	Op Amplifier	3041458	3	MC1458P1	04713
U6	U5				
U7	Quad, 2 INP OR Gate	3087432	1	DM74LS32	01295
U8	Digital Binary Counter	3074177	1	DM74177	01295
U9	Quad, 2INP, NAND Gate	3087400	3	DM74LS00	01295
U10	Dual 1-4 Demux	3084155	1	DM74LS155	01295
U11	Mulitibibrator	3009602	1	DM9602	01295
U12	U9				
U13	Dual, 4INP NAND Gate	3087420	1	DM74LS20	01295
U14	Quad, 2INP AND Gate	3087408	1	DM74LS08	01295
U15	U9				
U16	Liniar Op Amplifier	3043130	2	CA3130S	07263
U17	U16				
U18	Timer	3040555	1	NE555V	72136
U19	U4				
U20	U5				

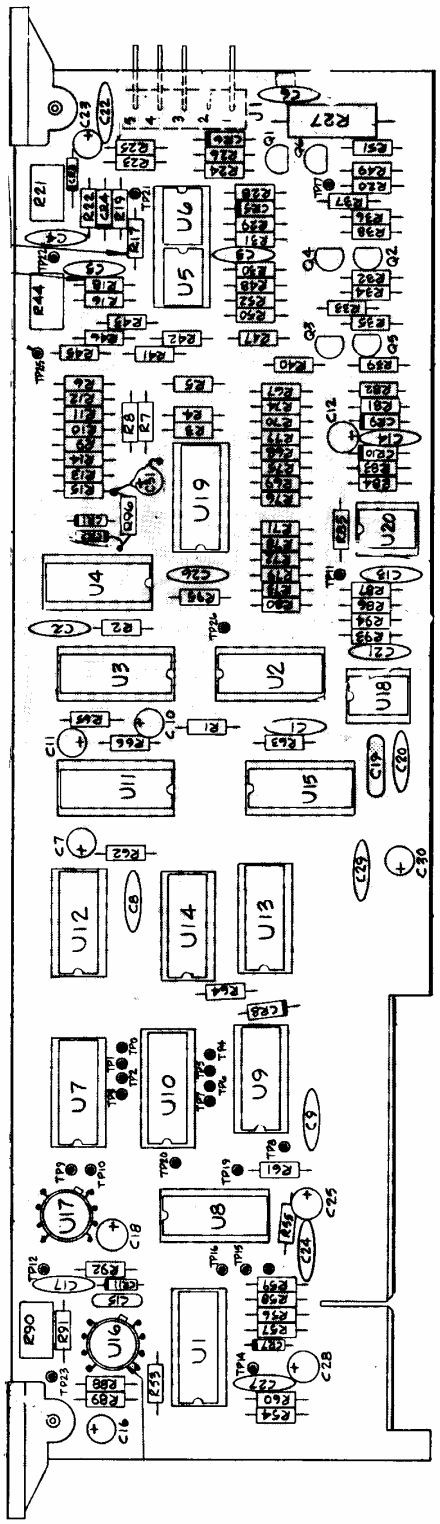
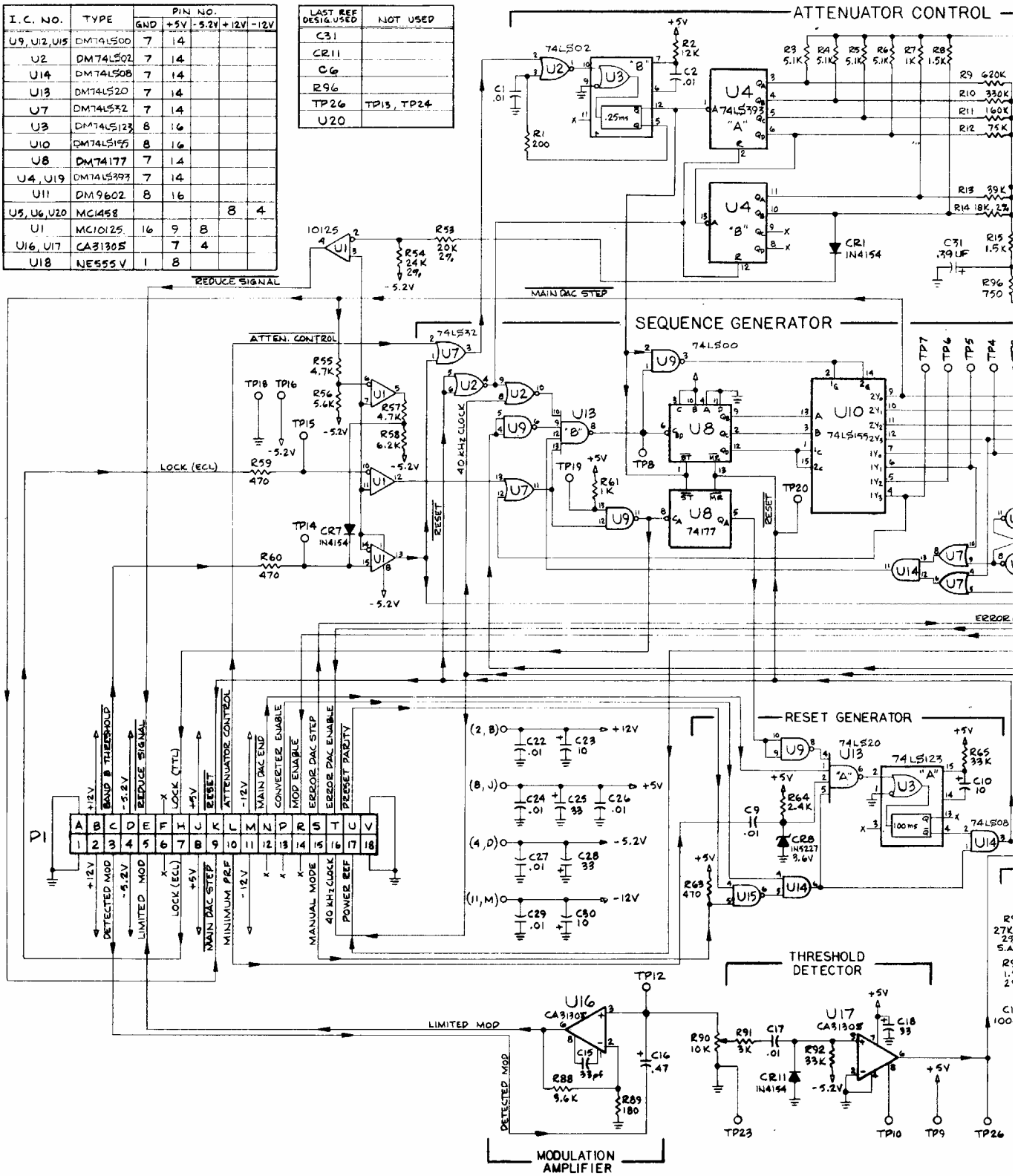


Figure 203-2. Converter Sequencer Component Locator

580010

I.C. NO.	TYPE	PIN NO. GND	+5V	-5.2V	+12V	-12V
U9, U12, U15	DM74LS00	7	14			
U2	DM74LS02	7	14			
U14	DM74LS08	7	14			
U13	DM74LS20	7	14			
U7	DM74LS32	7	14			
U3	DM74LS123	8	16			
U10	DM74LS155	8	16			
U8	DM74177	7	14			
U4, U19	DM74LS393	7	14			
U11	DM9602	8	16			
U5, U6, U20	MC1458				8	4
U1	MC10125	16	9	8		
U16, U17	CA3130S		7	4		
U18	NE555V	1	8			

LAST REF DESIG. USED	NOT USED
C31	
CR11	
C6	
R96	
TP26	TP13, TP24
U20	



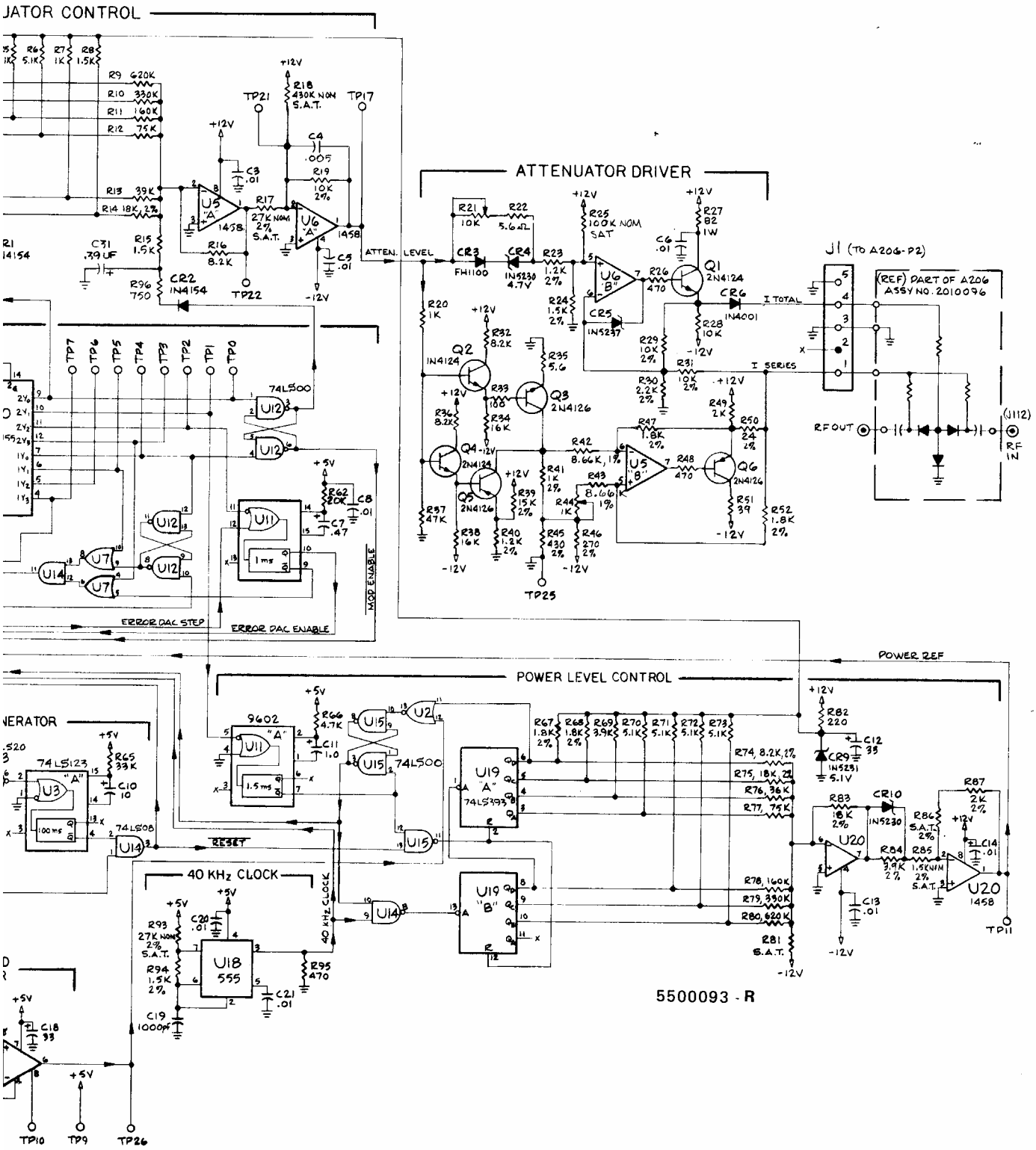


Figure 203-3. Converter Sequencer Schematic

A204
IF PROCESSOR
(2020094)

IF Processor A204 receives input from the Mixer (A205). It separates the Mixer output into IF and Video components, and processes the components to produce several outputs. The IF signal is amplified and limited for counting. The Video signal is used to produce the SIGNAL THRESHOLD, DETECTED MODULATION, and ATTENUATOR CONTROL signals directly. SIGNAL THRESHOLD is combined with the external INHIBIT INPUT to produce BAND B THRESHOLD. This signal, together with the IF signal, is used to determine LOCK.

IF AMPLIFIER

The IF component of the Mixer output is amplified in a six stage amplifier having an overall gain of 50 dB, and a bandwidth covering 100 MHz to 375 MHz. Stage 1 (Q1) is a common emitter amplifier with shunt feedback (R2). L2 and L3 provide high frequency shaping of the response. Stages 2, 3, and 4 (Q2-4) are similar to Stage 1. Gain is set by the emitter resistors. High frequency gain shaping is provided by the emitter RC network (R11, C8), and the collector inductor (L5).

Stages 5 and 6 are limiting amplifiers, each consisting of an amplifier (Q5, Q7) and an emitter follower (Q6, Q8). Each stage has a nominal gain of 10 dB, determined by the input and feedback resistors (R30, 34, 35). Capacitive bypassing (C25) is used for high frequency gain shaping. Diodes (CR1, 2) limit the final output still further.

VIDEO CIRCUITS

The Video output of the Mixer, representing the detected envelope of a microwave signal, is amplified by U1. R48 sets the voltage gain (nominally 100), while R51 nulls out any offset between the differential outputs at U1 pins 7 and 8.

Outputs of U1 are applied to a high speed differential amplifier (Q9, 10). Positive feedback from R61 converts this circuit to a Schmitt trigger. Q11 is an emitter follower used to drive the high speed ECL gates. The same outputs of U1 also differentially drive comparator U5 which forms the Attenuator Threshold Detector. Resistive biasing and feedback (R114–116, 118) set the trigger level of this circuit approximately 7dB above the Signal Threshold Detector level.

The remaining Video circuit is the 20 kHz amplifier consisting of Q12 and Q13. This circuit provides an additional voltage gain of 100 at frequencies near 20 kHz, and is used to detect the modulated comb lines during YIG leveling and centering operations.

IN-BAND DETECTOR

The In-Band Detector determines whether or not an IF signal exists within the correct frequency range and at sufficient level to obtain LOCK. The correct frequency range is the region from 100 MHz to 325 MHz. After LOCK, the upper end of this region is extended to 350 MHz.

A portion of the IF signal is coupled into an additional limiter section (Q14, 15) similar to the limiters in the IF Amplifier section. The output then drives two filter networks in parallel. The output of each network is detected (CR5, CR6), and compared in U2. Since input signal amplitude is held constant, the detected signals are determined entirely by the filter characteristics. One of the filter networks consists of a 100 MHz high-pass section (C51-53,-L12) in series with a 325 MHz low-pass section (L13-16,-C54), thus forming a band-pass filter from 100-300 MHz.

The second network consists of a 100 MHz low-pass section (L17-19, C57) in parallel with a 325 MHz high-pass section (C58-60, L20, L21), forming a band reject filter from 100-325 MHz.

By comparing the outputs of these two networks in U2, a determination of the IF frequency is made. R95 is used to precisely set the crossover frequency. After LOCK is obtained, Q16 and Q17 are turned on, shorting out L16 and L21, and increasing the crossover point from 325 MHz to 350 MHz.

LOCK LOGIC

The LOCK logic determines whether or not the proper conditions exist to consider the Converter locked. The condition to obtain LOCK is that an In-Band signal (from U2 pin 9) appears within 70 nanoseconds of the appearance of BAND B THRESHOLD (at Q11 collector). Once this condition is met, the LOCK command is latched, and remains active until a loss-of-lock condition is obtained – that is: an In-Band signal is not received within 70 nanoseconds of BAND B THRESHOLD.

BAND B THRESHOLD is generated by combining CONVERTER THRESHOLD (from Q11) with the external INHIBIT INPUT. The INHIBIT INPUT is buffered by Q21 and Q22. The two signals are combined at pins 12 and 13 of OR gate U3.

The LOCK latch consists of two gates of U4 with the output at U4 pin 14. The set input to this latch (U4 pin 5) is driven by a 3-input NOR gate (U4). The latch is set when all three inputs of the NOR gate are simultaneously low. R107 and C66 provide a 70 nanosecond delayed BAND B THRESHOLD to one input, while the inverted signal without a delay is applied to the second input. An inverted IN-BAND signal is applied to the third input. Thus a 70 nanosecond interval exists after BAND B THRESHOLD occurs, during which the LOCK latch may be set. The reset input to the latch is also a 3-input gate (U3), connected so IN-BAND must occur within 70 nanoseconds or the latch will be reset. If IN-BAND drops out while BAND B THRESHOLD remains (at any point in time after the 70 nanosecond interval), the latch is immediately reset.

A204 IF PROCESSOR

- 2020094 - V

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A204	IF Processor	2020094	1	EIP	34257
C1	Mica, 27pF, 5%, 500V	2250012	2	DM15 - 270J0	72136
C2	C1				
C3	Cer, .01μF, 20%, 1KV	2150003	25	TG - S10	72136
C4	C3				
C5	Cer, .001μF, 20%, 1KV	2150001	17	5GA - D10	56289
C6	C3				
C7	C3				
C8	Mica, 15pF, 5%, 500V	2550028	3	DM15 - 150J0	72136
C9	C3				
C10	C3				
C11	C5				
C12	C3				
C13	C3				
C14	C8				
C15	C3				
C16	C5				
C17	C3				
C18	C3				
C19	C8				
C20	C5				
C21	Mica, 10pF, 5%, 500V	2250001	3	DM15 - 100D0	72136
C22	C5				
C23	C3				
C24	C5				
C25	C3				
C26	C5				
C27	C5				
C28	C21				
C29	C5				
C30	C3				
C31	C5				
C32	Mica, 47pF,	2250017	1	DM15 - 470J	72136
C33	S.A.T.				
C34	C5				
C35	Cer, 6.8pF NPO, 500V	2160014	3	301000C0H0689J	72982
C36	Tant, 33μF, 10%, 10V	2300015	3	TAG20 - 33/10	14433
C37	C3				
C38	Tant, 10μF, 20%, 25V	2300029	6	TAG20 - 10/25	14433
C39	C36				
C40	C38				
C41	C38				
C42	Tant, .47μF, 20%, 25V	230005	2	TAG20 - .47/35	14433
C43	C42				
C44	C38				

A204 IF PROCESSOR, continued 2020094 - V

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C45	C5				
C46	C21				
C47	C5				
C48	C3				
C49	C3				
C50	C5				
C51	Cer, 22pF, NPO, 500V	2160009	3	301000C0G0220J	72982
C52	C51				
C53	C51				
C54	Cer, 3.0pF, NPO, 500V	2160011	1	301000C0J0309C	72982
C55	C5				
C56	C35				
C57	Cer, 18pF, NPO, 500V	2160007	1	301000C0G0180J	72982
C58	Cer, 4.7pF, NPO, 500V	2160013	2	301000C0H0479C	72982
C59	C35				
C60	C58				
C61	Mica, 68pF, 5%, 500V	2250025	1	DM15-680J	72136
C62	C3				
C63	C3				
C64	Miac, 20pF, 5%, 500V	2250008	1	DM15 - 200J	72136
C65	Mica, 120pF, 5%, 500V	2250027	2	DM15 -127J	72136
C66	C65				
C67	C3				
C68	Mica, 39pF, 5%, 500V	2250016	2	DM15 - 390J	72136
C69	C68				
C70 thru C72	C3				
C73	C38				
C74	C3				
C75	C38				
C76	C3				
C77	C36				
C78	C5				
C79	C5				
CR1	Hot Carrier	2710016	2	5082-2835	28480
CR2	CR1				
CR3	Zener, 6.2V	2705234	2	IN5234	04713
CR4	CR3				
CR5 and CR6	Matched pair, FH1100	2710014	1	EIP 2710004	34257

A204 IF PROCESSOR, continued 2020094 - V

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
L1	0.1μH	3510001	1	DD - 0.10	72259
L2	Not Used				
L3 thru L9	Part of PCB				
L10	1.2μH	3510010	2	1025-22	99800
L11	L10				
L12	0.15μH	3510008	1	DD - 0.15	72259
L13 thru L16	Part of PCB				
L17	0.12μH	3510011	3	DD - 0.12	72259
L18	L17				
L19	L17				
L20 thru L21	Part of PCB				
Q1	NPN, RF	4710026	5	NE73432B	72136
Q2	Graded, RED	4710011	7	4705179	34257
Q3	Q2				
Q4	Q2				
Q5 thru Q8	Q1				
Q9	PNP, RF	4710039	4	A8T4261-18	01295
Q10	Q9				
Q11	Graded - YELLOW	4710012	1	4705179	34257
Q12	NPN, General Purpose	4704124	1	2N4124	04713
Q13	PNP, General Purpose	4704126	1	2N4126	04713
Q14	Q9				
Q15	Q9				
Q16	Q2				
Q17	Q2				
Q18	PNP, RF	4710010	3	MPS - H81	04713
Q19	Q2				
Q20	Q2				
Q21	Q18				
Q22	Q18				
R1	Met Ox, 1.3K NOM, S.A.T.	4130999	1	C4/2%/SAT	24546
R2	Met Ox, 200, 2%, 1/4 W	4130201	1	C4/2%/200	24546
R3	Met Ox, 620, 2%, 1/4 W	4130621	4	C4/2%/621	24546
R4	Met Ox, 56, 2%, 1/4 W	4130560	5	C4/2%/560	24546
R5	Met Ox, 2.4K, 2%, 1/4 W	4130242	4	C4/2%/242	24546
R6	Comp, 5.6, 5%, 1/4 W	4010596	9	RC07GF596J	81349

A204 IF PROCESSOR, continued -2020094 - V

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R7	R3				
R8	Met Ox, 910, 2%, 1/4 W	4130911	3	C4/2%/911	24546
R9	Not Used				
R10	CBN Film, 8.2, 5%, 1/2 W	4120008	6	R25-8.2 - 5%, 1/4 W	0000X
R11	R10				
R12	R4				
R13	R5				
R14	R6				
R15	R3				
R16	R8				
R17	R10				
R18	R10				
R19	R4				
R20	R5				
R21					
thru					
R23	R6				
R24	R3				
R25	R8				
R26	Not Used				
R27	R10				
R28	R10				
R29	Comp, 51, 5%, 1/4 W	4010510	2	RC07GF510J	81349
R30	Comp, 47, 5%, 1/4 W	4010470	4	RC07GF470J	81349
R31	Met Ox, 270, 2%, 1/4 W	4130271	5	C4/2%/271	24546
R32	Met Ox, 430, 2%, 1/4 W	4130431	1	C4/2%/431	24546
R33	Comp, 10, 5%, 1/4 W	4010100	3	RC07GF100J	81349
R34	R31				
R35	Met Ox, 220, 2%, 1/4 W	4130221	2	C4/2%/221	24546
R36	Met Ox, 820, 2%, 1/4 W	4130821	3	C4/2%/821	24546
R37	R6				
R38	R29				
R39	R30				
R40	R31				
R41	Met Ox, 150, 2%, 1/4 W	4130151	1	C4/2%/151	24546
R42	R33				
R43	R31				
R44	R35				
R45	R36				
R46	R6				
R47	Met Ox, 470, 2%, 1/4 W	4130471	3	C4/2%/471	24546
R48	Variable Cer, 1K	4250003	1	72XWR1K	73138
R49	R47				
R50	Comp, 330K, 5%, 1/4 W	4010334	1	RC07GF334J	81349
R51	Variable Cer, 10K	4250006	2	72XWR10K	73138
R52	Comp, 160, 5%, 1/2 W	4020161	2	RC20GF161J	81349

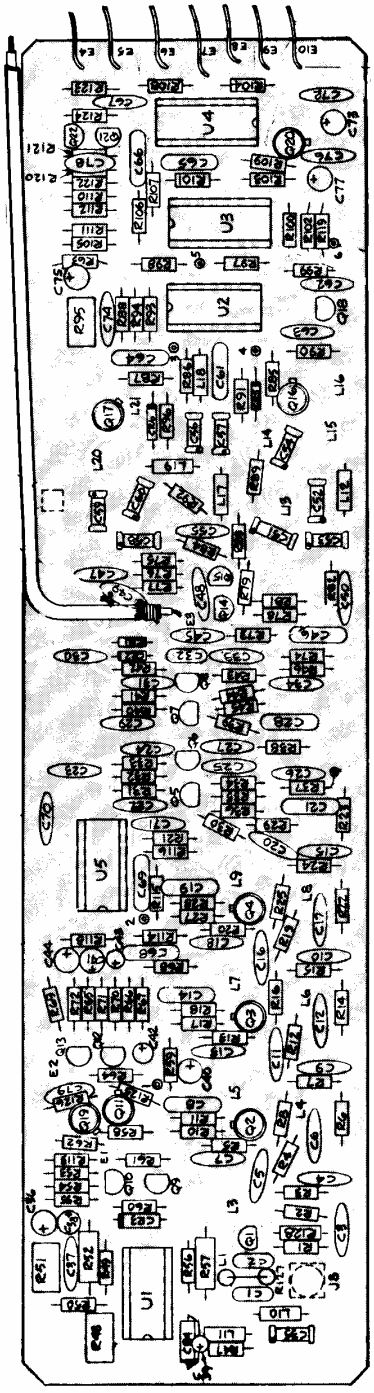
A204 IF PROCESSOR, continued 2020094 - V

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R53	R6				
R54	Met Ox, 100, 2%, 1/4 W	4130101	3	C4/2%/101	24546
R55	Met Ox, 1.6K, 2%, 1/4 W	4130162	1	C4/2%/162	24546
R56	Met Ox, 750, 2%, 1/4 W	4130751	1	C4/2%/751	24546
R57	R52				
R58	R5				
R59	R54				
R60	R54				
R61	Met Ox, 1K, 2%, 1/4 W	4130102	3	C4/2%/102	24546
R62	Met Ox, 240, 2%, 1/4 W	4130241	1	C4/2%/241	24546
R63	Comp, 180, 5%, 1/4 W	4010181	2	RC07GF181J	81349
R64	Comp, 4.3K, 5%, 1/4 W	4010432	2	RC07GF432J	81349
R65	R64				
R66	Comp, 430, 5%, 1/4 W	4010431	1	RC07GF431J	81349
R67	Comp, 13K, 5%, 1/4 W	4010133	1	RC07GF133J	81349
R68	Comp, 100, 5%, 1/4 W	4010101	4	RC07GF101J	81349
R69	R68				
R70	Comp, 620, 5%, 1/4 W	4010621	1	RC07GF621J	81349
R71	R68				
R72	Comp, 1K, 5%, 1/4 W	4010102	7	RC07GF102J	81349
R73	R63				
R74	Met Ox, 51, 2%, 1/4 W	4130510	1	C4/2%/510	24546
R75	R33				
R76	R47				
R77	R31				
R78	R30				
R79	Met Ox, 330, 2%, 1/4 W	4130331	1	C4/2%/331	24546
R80	Not Used				
R81	Comp, 820, 5%, 1/4 W	4010821	1	RC07GF821J	81349
R82	R6				
R83	Met Ox, 47, 2%, 1/4 W	4130470	2	C4/2%/470	24546
R84	R83				
R85	Comp, 3.3K, 5%, 1/4 W	4010332	2	RC07GF332J	81349
R86	R30				
R87	R85				
R88	Comp, 10K, 5%, 1/4 W	4010103	4	RC07GF103J	81349
R89	R4				
R90	Met Ox, 10K, 2%, 1/4 W	4130103	2	C4/2%/103	24546
R91	Met Ox, 43K, 2%, 1/4 W	4130433	2	C4/2%/433	24546
R92	R4				
R93	R90				
R94	R91				
R95	R51				
R96	Met Ox, 18K, 2%, 1/4 W	4130183	1	C4/2%/183	24546
R97	Met Ox, 1.3K, 2%, 1/4 W	4130132	1	C4/2%/132	24546
R98	Met Ox, 1.5K, 2%, 1/4 W	4130152	1	C4/2%/152	24546

A204 IF PROCESSOR, continued 2020094 - V

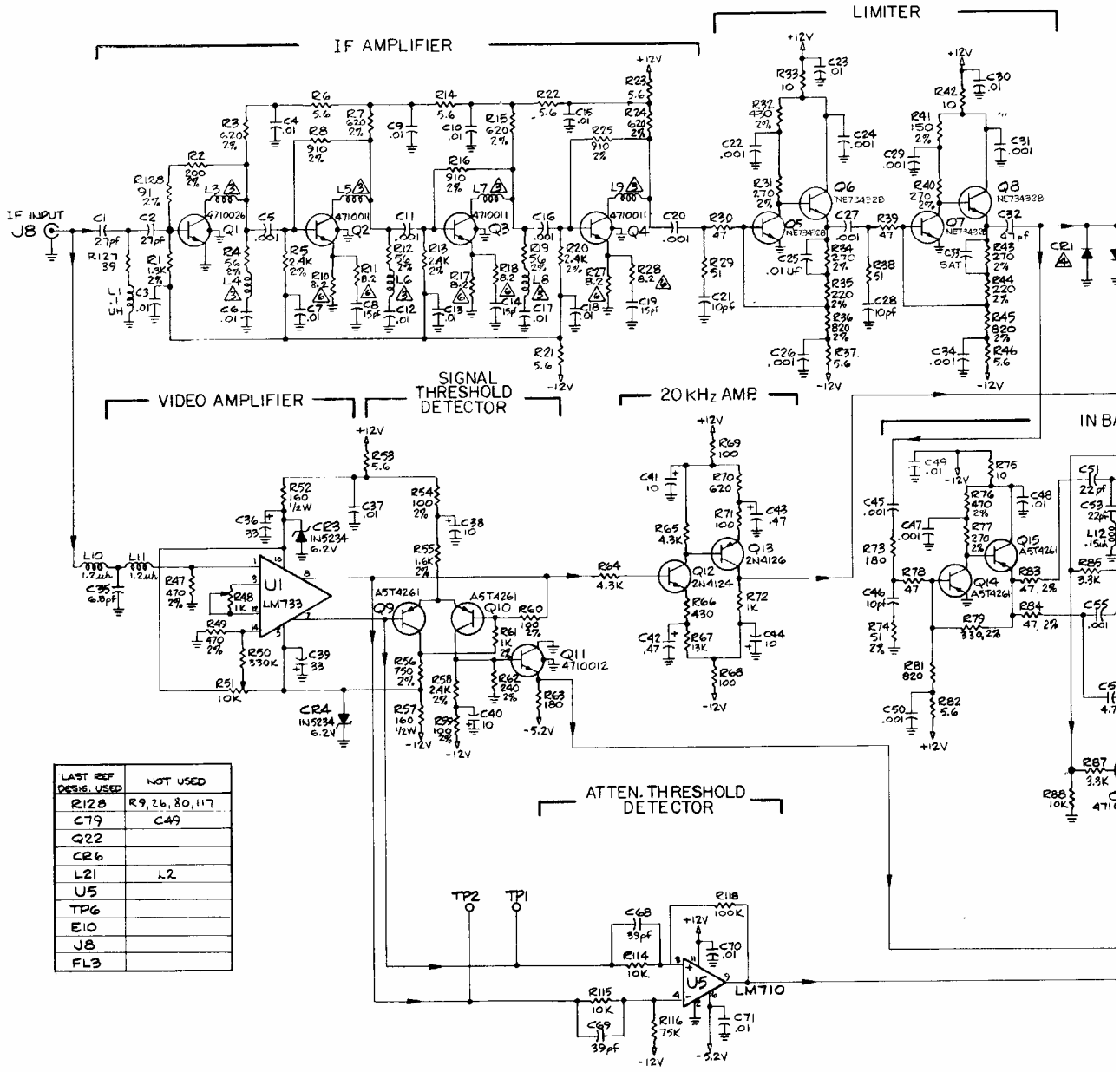
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R99	Comp, 4.7K, 5%, 1/4 W	4010472	1	RC07GF472J	81349
R100	Comp, 390, 5%, 1/4 W	4010391	3	RC07GF391J	81349
R101	R61				
R102	R72				
R103	R72				
R104	Comp, 20, 5%, 1/4 W	4010200	1	RC07GF200J	81349
R105	R100				
R106	R72				
R107	R61				
R108	R72				
R109	R72				
R110	R100				
R111	Comp, 220, 5%, 1/4 W	4010221	1	RC07GF221J	81349
R112	Comp, 110, 5%, 1/4 W	4010111	1	RC07GF111J	81349
R113	R68				
R114	R88				
R115	R88				
R116	Comp, 75K, 5%, 1/4 W	4010753	1	RC07GF753J	81349
R117	Not Used				
R118	Comp, 100K, 5%, 1/4 W	4010104	1	RC07GF104J	81349
R119	R88				
R120	Met Ox, 300, 2%, 1/4 W	4130301	1	C4/2%/301	24546
R121	R36				
R122	R72				
R123	Comp, 82, 5%, 1/4 W	4010820	1	RC07GF820J	81349
R124	Comp, 130, 5%, 1/4 W	4010131	1	RC07GF131J	81349
R125	Met Ox, 2K, 2%, 1/4 W	4130202	1	C4/2%/202	24546
R126	Met Ox, 120, 2%, 1/4 W	4130121	1	C4/2%/121	24546
R127	Comp, 39, 5%, 1/4 W	4010390	1	RC07GF390J	81349
R128	Met Ox, 91, 2%, 1/4 W	4130910	1	C4/2%/910	24546
U1	Diff. Video Amplifier	3040733	1	LM733CN	0000X
U2	Voltage Comparator	3050710	2	LM710CN	0000X
U3	Tri OR Gate	3110105	2	MC10105L	04713
U4	U3				
U5	U2				

PAGE LEFT BLANK INTENTIONALLY



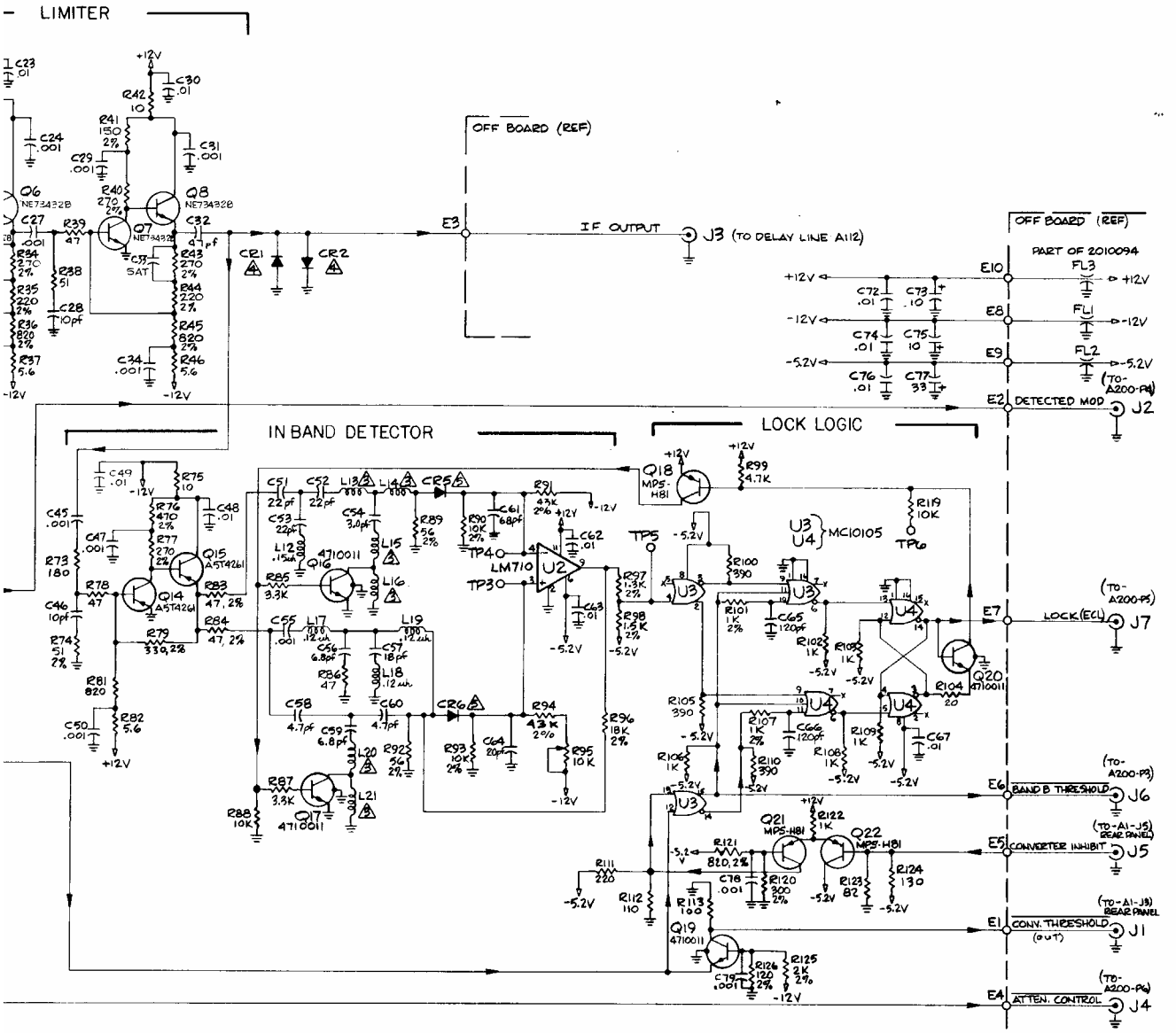
2020094 - V

Figure 204-1. IF Processor Component Locator



LAST REF DESIG. USED	NOT USED
R128	R9, 26, 80, 117
C79	C49
Q22	
CR6	
L21	L2
U5	
TP6	
E10	
J8	
FL3	

1. R10, R11, R17, R18, R27 & R28 ARE CARBON FILM, 1/4 W, 5%.
2. CR5 & CR6 ARE A MATCHED PAIR, P/N FH1100.
3. CR1 & CR2 ARE H.P. P/N 5082-2835.
4. INDUCTORS INDICATED ARE PART OF P.C. BOARD: L3 THRU L9, L13 THRU L16, L20 & L21.



5500094 - K

Figure 204-2. IF Processor Schematic

Section 9
Options

This section contains descriptions, schematic diagrams, parts lists and component location drawings for options used with the 451 Microwave Pulse Counter.

OPTIONS

P1 – Temperature Compensated Crystal Oscillator, TCXO.

P2 – Prescaler

P3 – Rear Panel Inputs

P4 – BCD/OUTPUT/REMOTE Programming

P5 – GPIB System Interface per IEEE Standard 488-1975

OPTION P1
TCXO

The P1 option is an additional temperature-compensated crystal oscillator that, when installed on the Reference Oscillator Buffer (A108) in place of the standard RTO, will offer extended stability and higher level of measurement precision. Aging rate of $<|3\times10^{-7}|$/ month and a temperature stability of $<|3\times10^{-5}|$ over the range of 0° C to 50° C are standard. With the P1 option the temperature instability is reduced to $<|2\times10^{-6}|$. By calibration against a frequency standard, this error can be made less than one count and thus becomes insignificant.

P1 option is shown in Section 108.

OPTION P2
PRESCALER

This option permits the measurement of pulse modulated signals that lie within the frequency range of 300 MHz to 950 MHz, and with pulse widths as narrow as 100 nsec.

The Prescaler divides the input signal frequency by four before applying it to the High Frequency board (A106). Simultaneously, the gate time is extended by a factor of four, to allow display of the true input frequency.

CIRCUIT DESCRIPTION

Input RF power is amplified in broadband limiting amplifiers Q3 and Q4, and applied to U3 which divides the frequency by four. Emitter follower Q5 provides sufficient drive current for 50 ohms lines.

The output of Q3 and Q4 is also applied to a threshold trigger circuit. The envelope is first detected by C6, CR1, and CR2, before driving Schmitt trigger U1A. Threshold of the Schmitt circuit is adjusted to trigger only at signal levels that are sufficiently large enough to permit reliable counting in the divide by four circuitry of U3.

Power for U3 is switched on or off by the circuitry associated with Q6-Q10. When the Band A Select line goes to a TTL high, differential amplifier Q6/7 saturates Q9 and allows the base of Q8 to become biased at approximately -7.4 volts. Q8 and Q10 are emitter followers that supply the -7.4 volts at approximately 60 ma to U3.

The remainder of the circuitry is interface switching logic to provide the indicated control signals. When the Band A Select line goes to a TTL high, U2A is enabled and passes the Band A signal threshold to the SIGNAL THRESHOLD output connector on the rear panel of the counter. Conversely, when the line is a TTL low, the Converter threshold signal is passed through U2B to the connector.

If the INHIBIT INPUT is either open, an ECL low (-1.7 V), or -1 volt from a 50 ohm source, U1C enables U2C allowing passage of the threshold trigger to the Gate Generator.

Refer to the specifications in Section 1.

PAGE LEFT BLANK INTENTIONALLY

A109 PRESCALER

2020079 - S

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A109	Prescaler	2020079	1	EIP	34257
C1	Cer, .01μF, 20%, 100V	2150003	12	TG - S10	56289
C2 thru C5	C1				
C6	Chip, 10pF, 5%, 50V	2100011	3	ATC100A100JC50	29990
C7	Chip, .001μF, 20%, 50V	2100002	13	VJ1210A102MF	95275
C8	Mica, 7pF, 5%, 500V	2250031	1	DM15CD7R0J	72136
C9	Cer, 6.8 pF, NPO, 500V	2160014	2	301000C0H0689C	72982
C10	C9				
C11	Cer, 20pF, NPO, 500V	2160016	1	301000C0G0200J	72982
C12 thru C14	C7				
C15	C6				
C16 thru C23	C7				
C24	Mica, 20pF, 5%, 500V	2250008	1	DM-15-200J	72136
C25 thru C27	C1				
C28	Tant, 10μF, 20%, 25V	2300029	2	TAG 20-10/25	14433
C29	C1				
C30	Tant, 33μF, 20%, 10V	2300015	2	TAG 20-33/10-50	14433
C31	C1				
C32	C28				
C33	C1				
C34	C30				
C35	C1				
C36	C7				
C37	DISC, .001μF, 20%, 1KV	2150001	1	5GA-D10	56289
C38	Mica, 200pF, 5%, 500V	2250009	1	DM15201P	72136
C39	C6				
CR1	Hot Carrier	2710016	3	5082-2835	28480
CR2	CR1				
CR3	CR1				
Q1	RF Graded, Yellow	4710012	2	EIP	34257
Q2	Q1				
Q3	NPN, RF	4710024	2	BRF90	73445
Q4	Q3				
Q5	NPN, RF, SW	4710017	1	MMT3960	04713
Q6	PNP, General Purpose	4704126	2	2N4126	04713

A109 PRESCALER , continued 2020079 - S

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
Q7	Q6				
Q8	NPN, General Purpose	4704124	2	2N4124	04713
Q9	Q8				
Q10	PNP, Power				
R1	Met Ox, 82, 2%, 1/4 W	4130820	1	C4/2%/82	24546
R2	Met Ox, 130, 2%, 1/4 W	4130131	1	C4/2%/131	24546
R3	Comp, 2K, 5%, 1/4 W	4010202	2	RC07GF202J	81349
R4	Comp, 390, 5%, 1/4 W	4010391	5	RC07GF391J	81349
R5	R3				
R6	Met Ox, 220, 2%, 1/4 W	4130221	3	C4/2%/221	24546
R7	Met Ox, 3.3K, 2%, 1/4 W	4130332	2	C4/2%/332	24546
R8	Comp, 430, 5%, 1/4 W	4010431	2	RC07GF431J	81349
R9	Met Ox, 1K, 2%, 1/4 W	4130102	1	C4/2%/102	24546
R10	Met Ox, 680, 2%, 1/4 W	4130681	3	C4/2%/681	24546
R11	R4				
R12	R4				
R13	Met Ox, 100, 2%, 1/4 W	4130101	1	C4/2%/107	24546
R14	R6				
R15	R6				
R16	Met Ox, 1.3K, 2%, 1/4 W	4130132	1	C4/2%/132	24546
R17	R4				
R18	R4				
R19	Not Used				
R20	R8				
R21	R7				
R22	Not Used				
R23	Met Ox, 1.5K NOM	413999	1	C4/2%/S.A.T.	24546
R24	Met Ox, 180, 2%, 1/4 W	4130181	1	C4/2%/181	24546
R25	Met Ox, 51, 2%, 1/4 W	4130510	2	C4/2%/51	24546
R26	Met Ox, 3K, 2%, 1/4 W	4130302	1	C4/2%/302	24546
R27	Met Ox, 510, 2%, 1/4 W	4130511	1	C4/2%/511	24546
R28	R10				
R29	Met Ox, 12, 2%, 1/4 W	4130120	1	C4/2%/120	24546
R30	Met Ox, 430, 2%, 1/4 W	4130431	1	C4/2%/430	24546
R31	Met Ox, 470, 2%, 1/4 W	4130471	1	C4/2%/470	24546
R32	R25				
R33	Met Ox, 7.5K, 2%, 1/4 W	4130752	1	C4/2%/752	24546
R34	Not Used				
R35	Met Ox, 620, 2%, 1/4 W	4130621	2	C4/2%/621	24546
R36	R35				
R37	Met Ox, 270, 2%, 1/4 W	4130271	1	C4/2%/271	24546
R38	Met Ox, 360, 2%, 1/4 W	4130361	1	C4/2%/361	24546
R39	R10				
R40	Met Ox, 2K, 2%, 1/4 W	4130202	1	C4/2%/202	24546
R41	Met Ox, 3.9K, 2%, 1/4 W	4130392	1	C4/2%/392	24546

A109 PRESCALER, continued 2020079 - S

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R42	Comp, 1K, 5%, 1/4 W	4010102	1	RC07GF102J	81349
R43	Met Ox, 6.2K, 2%, 1/4 W	4130622	1	C4/2%/622	24546
R44	Met Ox, 4.7K, 2%, 1/4 W	4130472	1	C4/2%/472	24546
R45	Comp, 470, 5%, 1/4 W	4010471	2	RC07GF471J	81349
R46	R45				
R47	Comp, 4.3K, 5%, 1/4 W	4010432	1	RC07GF432J	81349
R48	Comp, 3.6K, 5%, 1/4 W	4010362	1	RC07GF362J	81349
R49	Comp, 10, 5%, 1/8 W	4000100	1	RC05GF100J	81349
R50	Comp, 5.6, 5%, 1/8 W	4000569	1	RC05GF569	81349
U1	Triple Line Receiver	3110216	1	MC10216L	04713
U2	Quad, 2 input AND Gate	3110104	1	MC10104P	04713
U3	UHF Center-Divide/4	3010617	1	SP8617B	0000X

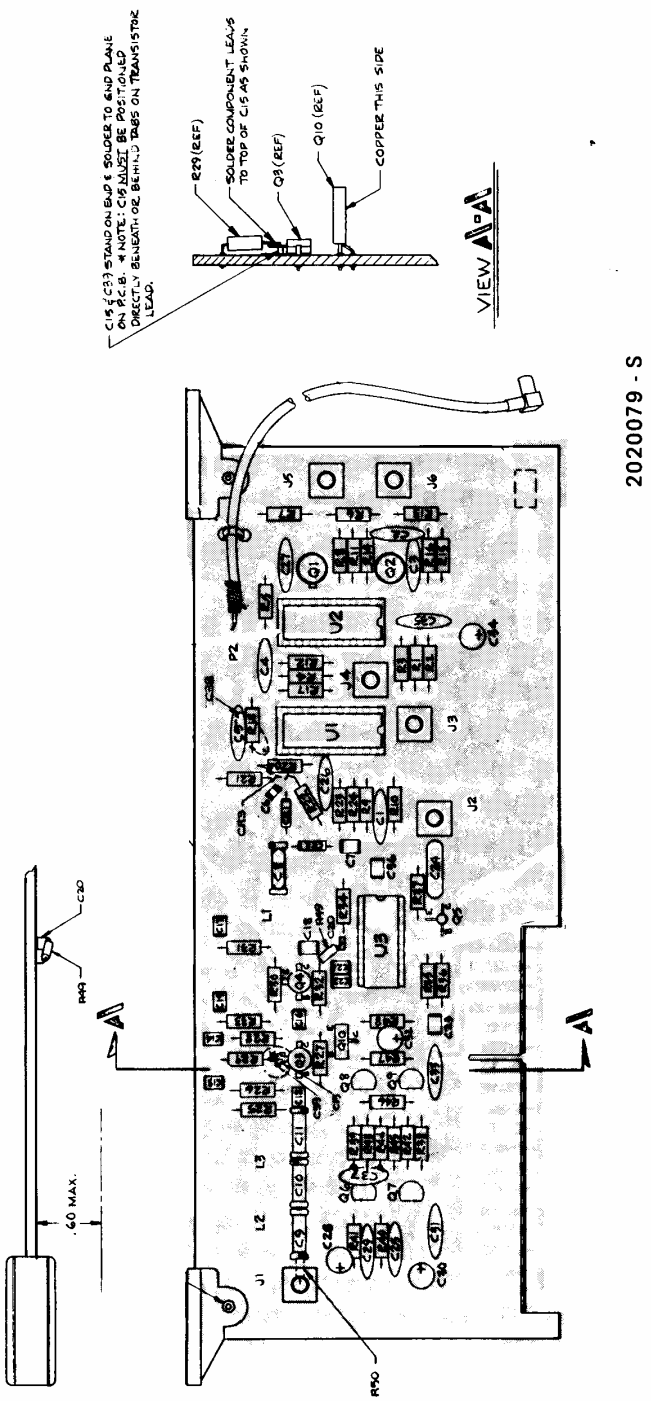
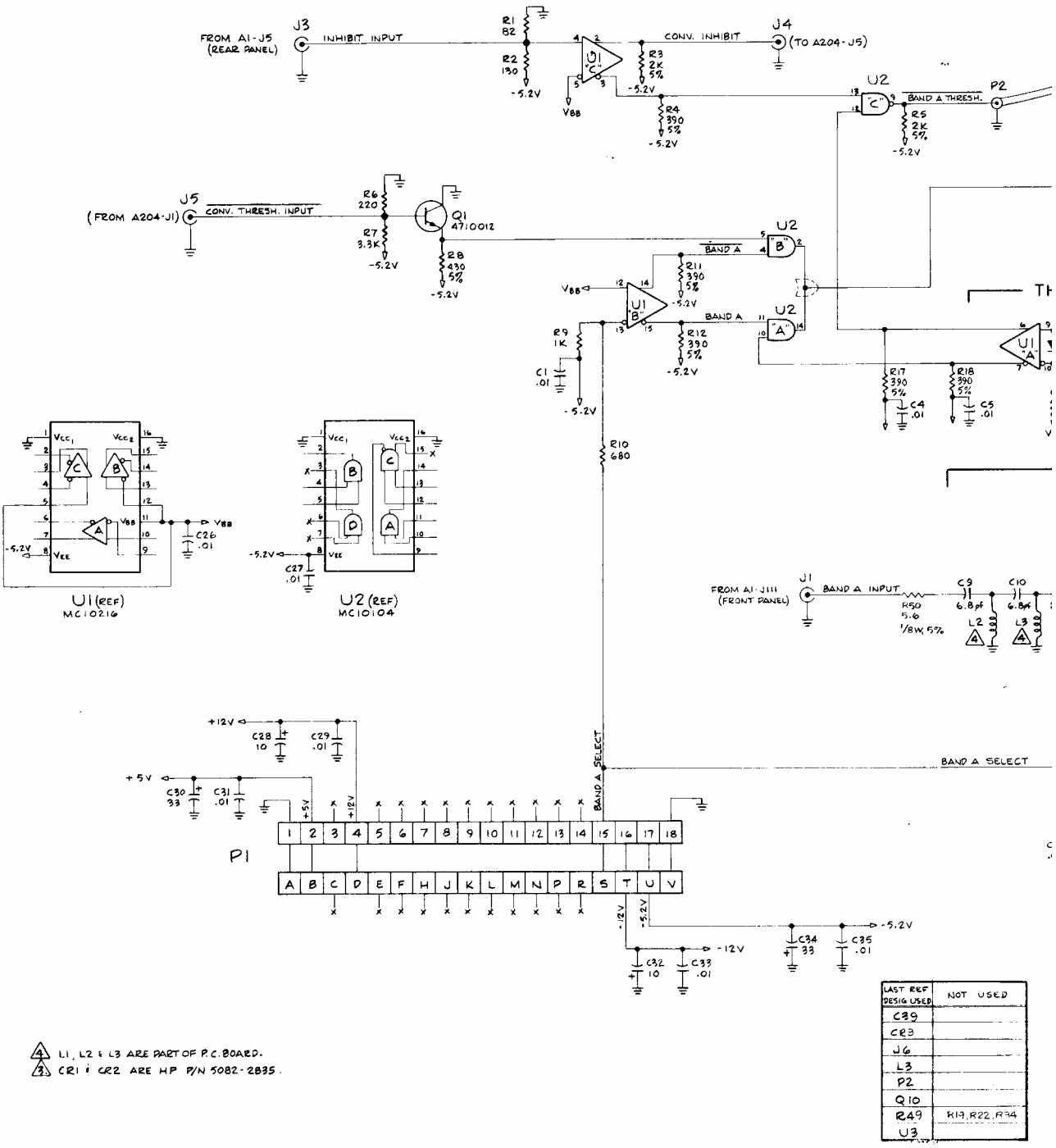
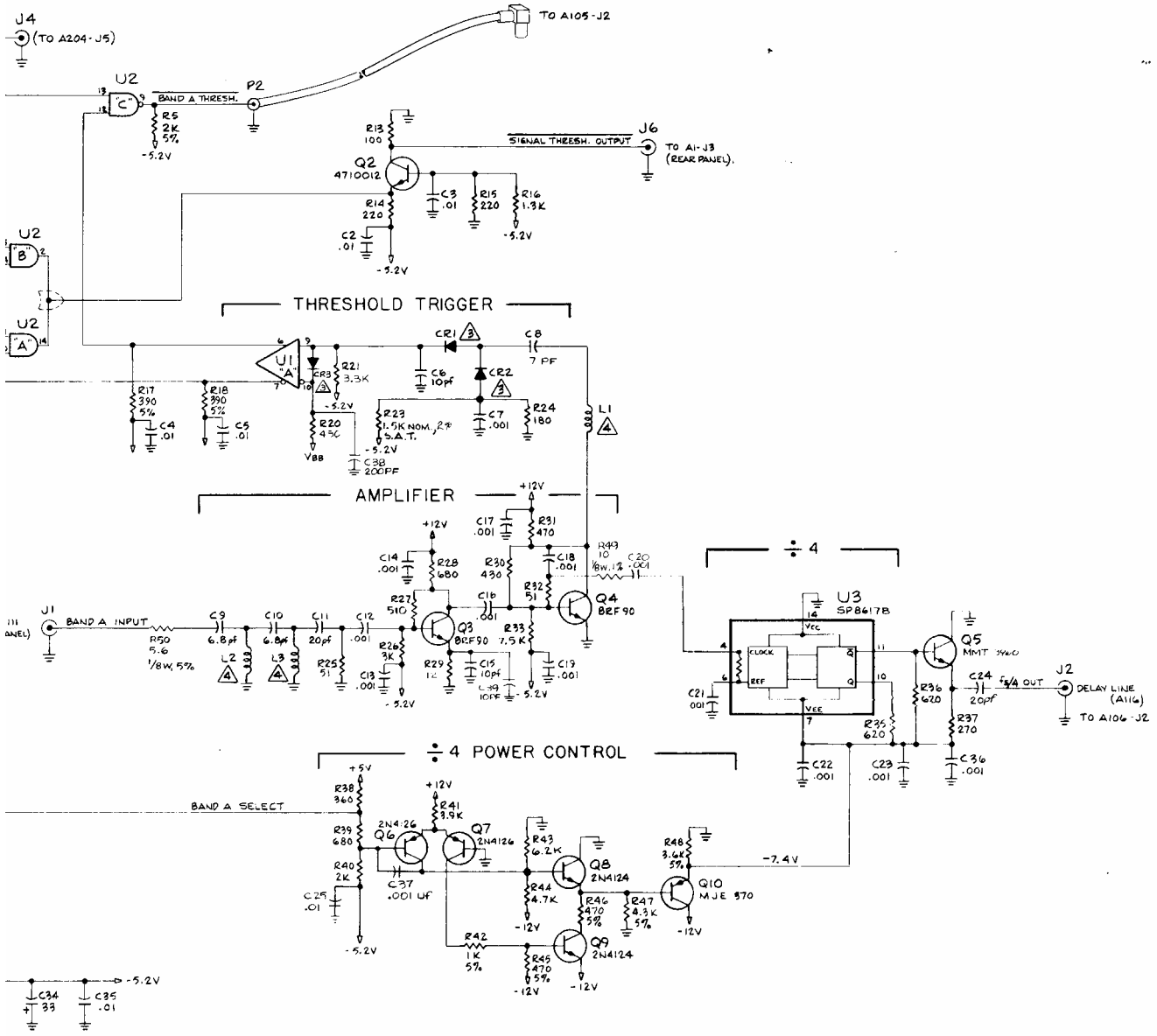


Figure P2-1. Prescaler Component Locator



LAST REF DESIG USED	NOT USED
C39	
CR3	
J6	
L3	
P2	
Q10	
R49	R19, R22, R34
U3	

4. L1, L2 & L3 ARE PART OF P.C. BOARD.
3. CR1 & CR2 ARE HP P/N 5082-2835.



LAST REF DESIG USED	NOT USED
C39	
CR3	
J6	
L3	
P2	
Q10	
R49	R19, R22, R34
U3	

5500079 - L

Figure P2-2. Prescaler Schematic

OPTION P3
REAR PANEL INPUT

For this option, the Converter is switched end-for-end, with the Band B input connector projecting through the existing opening the rear panel, and with certain cables re-routed and changed in length.

TO FIELD CHANGE BAND B TO REAR INPUT

1. Disconnect power cord, and remove both top and bottom covers from the counter.
2. Unplug all cables which connect Converter to Basic Counter. Note cable routing and connections.
3. Unscrew Converter tray retaining screws (from bottom of Counter).
4. Lift rear of Converter tray, and carefully slide Converter out of counter enclosure.
5. Turn Converter end-for-end, and insert the Band B connector through the hole in the rear panel labeled 925 MHz - 18 GHz.
6. Lower Converter carefully into counter enclosure, taking precautions not to pinch any wires or cables.
7. Install screws which hold Converter in enclosure, and reconnect cables unplugged in step 2. above.
8. Perform Incoming Operational Check described in Section 2 — Installation.
9. Apply a signal to the Band B input connector within the correct frequency and power limits, checking for proper operation of the Converter. Specifications remain identical to those for front panel operation.

TO FIELD CHANGE BANDS A AND B TO REAR INPUT

1. Disconnect power cord, and remove both top and bottom covers from the counter.
2. Unplug all cables which connect Converter to Basic Counter. Note cable routing and connections.
3. Unscrew Converter tray retaining screws (from bottom of Counter).
4. Lift rear of Converter tray, and carefully slide Converter out of counter enclosure.
5. Turn Converter end-for-end, and insert the Band B connector through the hole in the rear panel labeled 925 MHz - 18 GHz.
6. Lower Converter carefully into counter enclosure, taking precautions not to snag or pinch any wires or cables.
7. Install screws which hold Converter in enclosure.
8. Locate Double Delay Line Assembly A116. Note that three cables exit from under one end of the cover, and one cable (to A204J3) exits from under the other end of the cover. Loosen, but do not remove the screws holding the Delay Line cover in place. Re-route the cable to A204J3 so it exits from the same end as the remaining three cables. Tighten the Delay Line cover screws.
9. All three plug-in cables to the Prescaler PC board (A109) must be replaced with those of a different length as follows: Replace short W30 cable (A109J1 - A1J111) with long W30 cable (with BNC connector mounted on rear panel); replace short W31 cable (A109J5 - A204J1) with long W31 cable; replace long W32 cable (A109J4 - A204J5) with short W32 cable.
10. Reconnect all cables unplugged in steps 2. and 9.
11. Perform Incoming Operational Check described in Section 2 — Installation.
12. Apply a signal to the Band B input connector within the correct frequency and power limits, checking for proper operation of the Converter. Specifications remain identical to those for front panel input.
13. Apply a signal to the Band A input connector within the correct frequency and power limits, checking for proper operation of the Prescaler. Specifications remain identical to those for front panel input.

OPTION P4
BCD OUTPUT/REMOTE PROGRAMMING

BCD output, remote programming, and YIG preset, are the three basic functions provided by this option. Circuitry to accomplish these functions is contained on PC board A111, with connections made through rear panel REMOTE INPUT/OUTPUT connector A1J7. All inputs and outputs are TTL compatible. Each basic function will be described separately, with A1J7 pin assignments and functions shown in Figure P4-1. (Recommended mating connector for A1J7: Amphenol 57-30500, 50 pin male – EIP Part No. 2640003.)

BCD OUTPUTS

BCD formatted outputs to A1J7 correspond to the applied signal input frequency. A PRINT command output signal indicates the presence of valid data, while an INHIBIT input prevents the data from being altered. Both PRINT and INHIBIT signals are active high.

BCD information from High Frequency board A106 enters A111 via J5 and J6. U1 through U5 buffer the information and supply it via P1 to A1J7.

YIG PRESET

YIG preset information is supplied to the counter from two sources, depending upon the status of the Local/$\overline{\text{Remote}}$ line. In the Local mode, preset information comes from the front panel thumbwheel and MAN SELECT/AUTO SWEEP switches. In the $\overline{\text{Remote}}$ mode, preset information is obtained via A1J7, and controlled by the status of the Conv Man/$\overline{\text{Auto}}$ line. Increments of the 200 MHz may be programmed using the standard 1-2-4-8 BCD code.

REMOTE PROGRAMMING

Except for POWER ON/OFF and SAMPLE RATE, all front panel switch functions can be remotely controlled. Additional remotely programmable functions which are in continuous operation and are unaffected by the status of the Local/$\overline{\text{Remote}}$ line, are: $\overline{\text{Fast Cycle}}$, Cycle Counter, and Pulse Reset. $\overline{\text{Fast Cycle}}$ bypasses the display delay generator and over-rides the SAMPLE RATE control. Cycle Counter is a capacitive-coupled input signal to reset the Basic Counter and initiate a new reading. Pulse Reset triggers a one-shot to reset the Counter and Converter.

U6 through U9 are quad 2-input multiplexers which are selected by the Local/$\overline{\text{Remote}}$ line to provide data from either the front panel switches (Local mode), or from the rear panel connector A1J7 ($\overline{\text{Remote}}$ mode). R6-R9 and U3 act as an input buffer for the INHIBIT line, thus allowing operation from 0 to +50 volts. CR1 and CR2 act as clamping diodes.

Pin No.	Function	Pin No.	Function	Pin No.	Function
1	10^4 A	18	$\overline{\text{Preset 1 GHz}}$	35	10^8 D
2	10^4 B	19	$\overline{\text{Preset 0.4 GHz}}$	36	10^9 C
3	10^5 A	20	Conv. Man/$\overline{\text{Auto}}$	37	10^9 D
4	10^5 B	21	Cycle Counter	38	10^{10} C
5	10^6 A	22	$\overline{\text{Fast Cycle}}$	39	+5 Vdc Ref.
6	10^6 B	23	$\overline{\text{1 MHz}}$ Resolution	40	Print Command
7	10^7 A	24	$\overline{\text{Band A}}$	41	$\overline{\text{Preset 8 GHz}}$
8	10^7 B	25	Local/$\overline{\text{Remote}}$	42	$\overline{\text{Preset 2 GHz}}$
9	10^8 A	26	10^4 C	43	$\overline{\text{Preset 0.8 GHz}}$
10	10^8 B	27	10^4 D	44	$\overline{\text{Preset 0.2 GHz}}$
11	10^9 A	28	10^5 C	45	$\overline{\text{Hold}}$
12	10^9 B	29	10^5 D	46	$\overline{\text{Test}}$
13	10^{10} A	30	10^6 C	47	$\overline{\text{Reset}}$
14	10^{10} B	31	10^6 D	48	$\overline{\text{100 kHz}}$ Resolution
15	Inhibit	32	10^7 C	49	Pulse Reset
16	$\overline{\text{Preset 10 GHz}}$	33	10^7 D	50	Ground
17	$\overline{\text{Preset 4 GHz}}$	34	10^8 C		

FIGURE P4-1. A1J7 CONNECTOR PIN ASSIGNMENTS

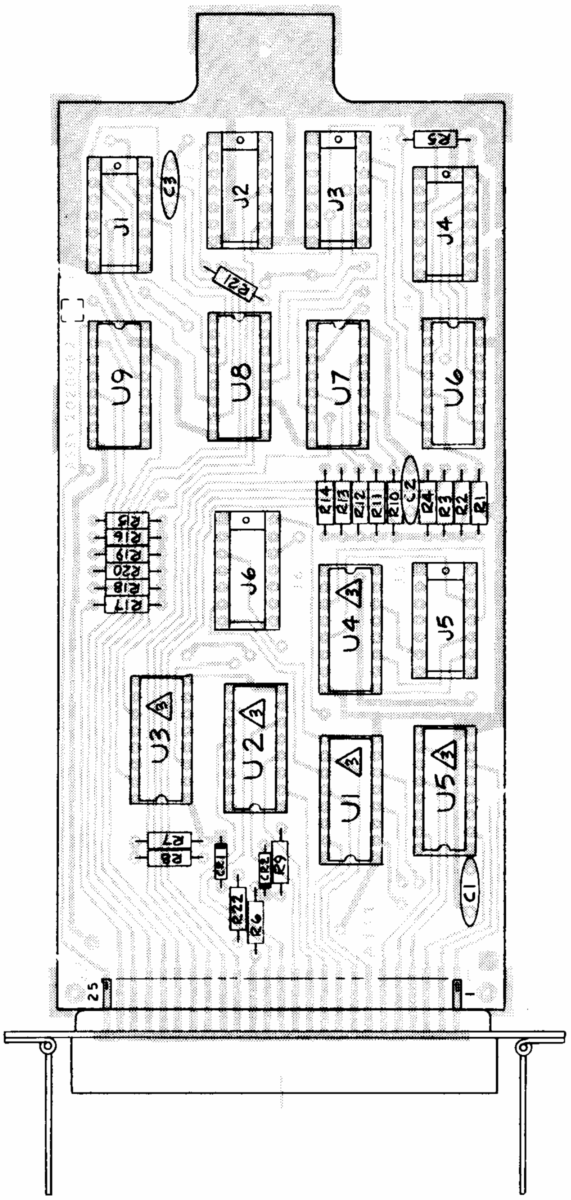
NOTES

1. The 10^4 bit is the least significant bit, and corresponds to the 10 kHz output. A, B, C, and D are the 1, 2, 4, and 8 bits of each BCD digit.
2. "Barred" commands ($\overline{\text{Hold}}$, $\overline{\text{Test}}$, etc.) are active low.
3. The command $\overline{\text{"Hold"}}$ retains the reading until manually reset. $\overline{\text{"Test"}}$ provides the same information as the front panel TEST switch. $\overline{\text{"Reset"}}$ overrides the SAMPLE RATE/HOLD control, resets the display to zero, and initiates a new reading. $\overline{\text{"100 kHz"}}$ and $\overline{\text{"1 MHz"}}$ set the resolution in the same manner as the front panel RESOLUTION switches. $\overline{\text{"Band A"}}$ places the counter in the Band A (Prescaler) range: 300 MHz - 950 MHz.

A111 BCD/REMOTE PROGRAMMING

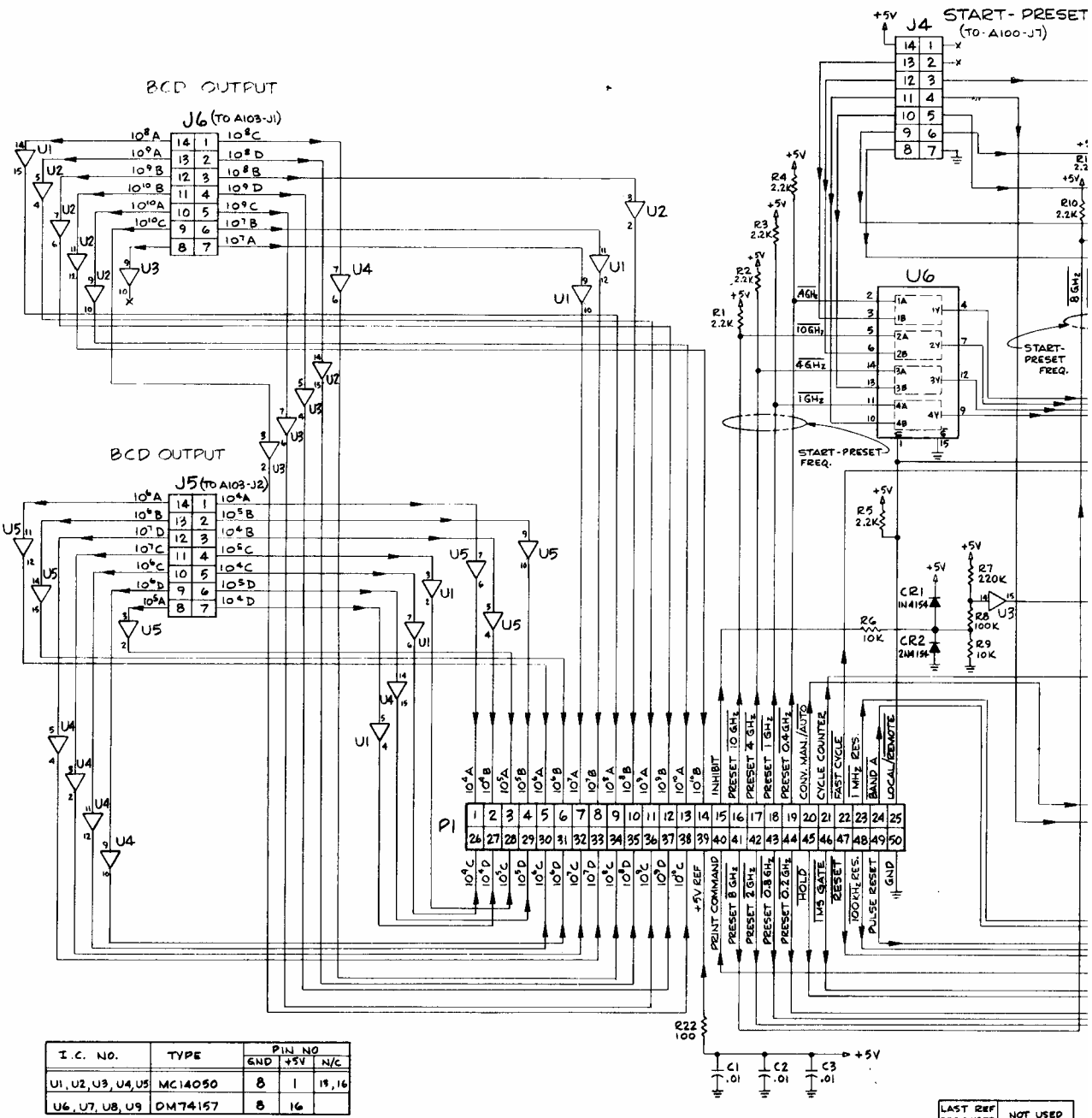
2020082 - F

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A111	BCD/Remote Programming	2020082	1	EIP	34257
C1	Cer, .01μF, 20%, 100V	2150003	3	TG - S10	56289
C2	C1				
C3	C1				
CR1	General Purpose	2704154	2	IN4154	07263
CR2	CR1				
R1	Comp, 2.2K, 5%, 1/4 W	4010222	16	RC07GF222J	81349
R2 thru R5	R1				
R6	Comp, 10K, 5%, 1/4 W	4010103	2	RC07GF103J	81349
R7	Comp, 220K, 5%, 1/4 W	4010224	1	RC07GF224J	81349
R8	Comp, 100K, 5%, 1/4 W	4010104	1	RC07GF104J	81349
R9	R6				
R10 thru R20	R1				
R21	Comp, 150, 5%, 1/4 W	4010151	1	RC07GF151J	81349
R22	Comp, 100, 5%, 1/4 W	4010101	1	RC07GF101J	81349
U1	Hex Buffer, Non-Invert	3114050	5	MC14050CP	04713
U2 thru U5	U1				
U6	Quad, 2 INP Multiplexer	3074157	4	DM74157	0000X
U7 thru U9	U6				



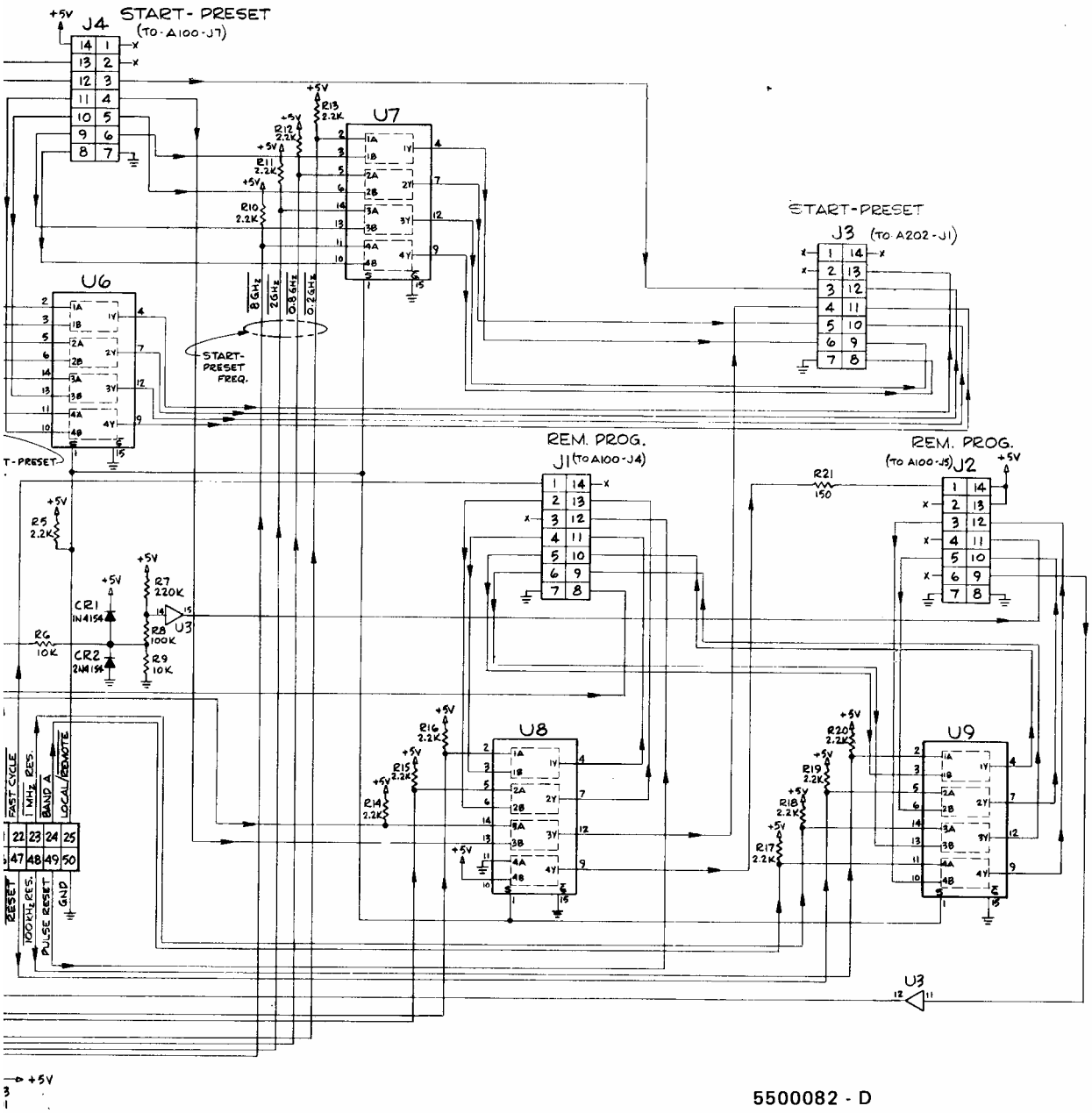
2020082 - F

Figure P4-2. BCD Output / Remote Programming Component Locator



I.C. NO.	TYPE	PIN NO		
		GND	+5V	N/C
U1, U2, U3, U4, U5	MC14050	8	1	13, 16
U6, U7, U8, U9	DM74157	8	16	

LAST REF DESIG. USED	NOT USED
C3	
CR2	
J6	
R22	
U9	



5500082 - D

LAST REF DESIG. USED	NOT USED
C3	
CR2	
J6	
R22	
U9	

Figure P4-3. BCD Output / Remote Programming Schematic

OPTION P5
GENERAL PURPOSE INTERFACE BUS

GENERAL

Option P5, the EIP General Purpose Interface Bus (GPIB), permits operation of an EIP 451 Microwave Pulse Counter from a data bus which conforms to the IEEE Standard Digital Interface for Programmable Instrumentation – IEEE STD 488-1975.

This option allows the user to program all the counter's front panel switches except for SAMPLE RATE adjustment. In addition, other functions that can be programmed via the GPIB include:

1. YIG Presets
2. Data Output Format (two types)
3. Normal or Fast Cycle Operation
4. Counter Reset

OPERATION

The counter may be used On Line or Off Line as selected by switch AM121S7 (on counter rear panel). On Line operation (counter connected to interface bus system) enables the counter to be programmed by sending any combination of 19 device dependent commands during the counter's LISTEN mode of operation. Device independent commands are received by the counter at any time during its operation. NOTE: The counter will ignore any device dependent or independent command for which it was not designed to respond. When all commands have been received and the counter is addressed to TALK, data is continuously transmitted in compliance with the IEEE STD 488-1975 Handshake Process to those devices addressed to LISTEN. The transmitted data has two output formats: scientific exponent or zero exponent, either of which can be selected by the programmer.

Off Line operation (counter not connected to the interface bus system), allows the counter to transmit ASCII coded data in bit parallel, byte serial form. BCD data may be extracted from this ASCII coded data if desired. Output rate and output data format (scientific or zero exponent), may be continuously controlled.

When not addressed to TALK or LISTEN, the counter monitors the bus for instructions. In all three modes: TALK, LISTEN, or MONITOR, the counter display is updated.

IMPLEMENTED INTERFACE FUNCTIONS:

SH1	Source Handshake function
AH1	Accepter Handshake function
T1	Talker function, subset T1
SR1	Service Request function, subset SR1
L4	Listener function, subset L4
RL2	Remote/Local function, subset RL2
DC1	Device Clear function, includes SDC (Selected Device Clear)

Timing pecularities encountered with some GPIB controllers may produce apparent handshake problems. Specifically, the PET, HP1000 and some Digital Equipment Computers may evidence this condition. If you should encounter any interface problems, please contact EIP customer service for assistance.

INTERFACE CHARACTERISTICS

NOTE: For complete details on electrical, mechanical, and timing requirements, refer to IEEE STD 488-1975.

BUS SIGNAL LINES

DIO1-DIO8 – DATA INPUT/OUTPUT Lines 1-8. Message bytes are transmitted on these lines in bit-parallel, byte-serial form, asynchronously, and usually in a bi-directional manner.

DAV – DATA VALID. This signal is used to indicate whether data on the DIO lines is available.

NRFD – NOT READY FOR DATA. This line indicates whether or not the device is ready to accept data.

NDAC – NOT DATA ACCEPT. This line is used to indicate whether or not the device has accepted the data sent to it on the DIO lines.

ATN – ATTENTION. This line indicates how data on the DIO lines is to be interpreted, and which devices must respond to the data.

IFC – INTERFACE CLEAR. This line is used to place the interface system, and those devices connected to it, in a known quiescent state.

SRQ – SERVICE REQUEST. This line is used to request service from the controller.

REN – REMOTE ENABLE. This line is used by the controller (in conjunction with other messages), to place the counter in the remote mode.

EOI* – END or IDENTIFY. This line is used to indicate the end of a data transfer or, with the ATN line, to execute a polling sequence.

** This line is not used by the counter, and is not active.*

Connector AM120P1 is used to connect the counter to the interface bus system. Pin assignments are:

CONTACT	SIGNAL LINE	CONTACT	SIGNAL LINE
1	DIO 1	13	DIO 5
2	DIO 2	14	DIO 6
3	DIO 3	15	DIO 7
4	DIO 4	16	DIO 8
5	EOI	17	REN
6	DAV	18	Gnd, (6)*
7	NFRD	19	Gnd, (7)*
8	NDAC	20	Gnd, (8)*
9	IFC	21	Gnd, (9)*
10	SRQ	22	Gnd, (10)*
11	ATN	23	Gnd, (11)*
12	Shield	24	Gnd, LOGIC

**NOTE: Gnd(n) refers to the signal ground return of the referenced pin.*

BUS LOGIC LEVELS

NOTE: All signals use negative-true logic, with a low equal to Logic 1.

RECEIVER SPECIFICATIONS

Low State: Input Voltage $\leq$ + 0.8 V

High State: Input Voltage $\geq$ +2.0 V

Hysteresis: $V_{+pos} - V_{+neg} \geq + 0.4$ V

$V_{+pos} \geq + 2.0$ V

$V_{+neg} \leq + 0.8$ V

DRIVER SPECIFICATIONS

Low State: Output Voltage $\leq$ + 0.4 V at 48 mA

High State: Output Voltage $\geq$ + 2.4 V at 5.2 mA

NOTE: Output drivers are tri-state devices, with a divider network of 3K ohms to +5 V, and 6.2 K to ground. Tri-state bus divider voltage: $+ 2.6 \text{ V} \leq V_d \leq + 3.7$ V.

DATA TRANSMISSION RATE

The data transmission rate is defined as the number of bytes per second (1 byte = 8 bits) at which data is transmitted under the Source Acceptor Handshake process.

Sample rate is defined as the number of complete, formatted frequency readings that can be taken with a specific resolution and gate time selected by the user.

Sample rates that can be attained by the counter while in FAST CYCLE operation. Data transmission rate is 2850 bytes/second (all resolutions and all bands). Data sample rate is in readings/second. The maximum rates are:

	RESOLUTION $\geq$ 10 kHz (readings per second)
Band A:	145
Band B:	145

NOTE: The actual data transmission rate and sample rate is determined by the slowest device connected to the system.

ADDRESS ASSIGNMENT

TALK and LISTEN addresses are selected by switches AM121S1 through S7 (counter rear panel). When power is turned on, the settings of these switches determine which TALK address and corresponding LISTEN address will be assigned to the counter. If at any time after power is turned on, it becomes necessary to change the address assignment, the new address is set into the switches, and the programmer then executes an SDC or DCL command assigning the new address to the counter. The SDC command is issued by addressing the counter with its present address (not the new address to be assigned).

Thirty-one TALK/LISTEN address assignments may be made in this manner. NOTE: The TALK/LISTEN address must not be assigned to any device on the bus; these addresses are reserved for unlisten/untalk commands.

					ASCII TALK		ASCII LISTEN
S1	S2	S3	S4	S5	Address Character	▸	Address Character
1	1	1	1	0	—		?

TALK/LISTEN address combinations and their corresponding ASCII character codes, and their decimal equivalents, which can be assigned to the counter are shown in Figure P5-1.

ADDRESS SWITCH SETTING S1	S2	S3	S4	S5	ASCII LISTEN ADDRESS CHARACTER	ASCII TALK ADDRESS CHARACTER	DECIMAL TALK/LISTEN ADDRESS *
0	0	0	0	1	SP	@	00
1	0	0	0	1	!	A	01
0	1	0	0	1	"	B	02
1	1	0	0	1	#	C	03
0	0	1	0	1	$	D	04
1	0	1	0	1	%	E	05
0	1	1	0	1	&	F	06
1	1	1	0	1	'	G	07
0	0	0	1	1	(	H	08
1	0	0	1	1	)	I	09
0	1	0	1	1	*	J	10
1	1	0	1	1	+	K	11
0	0	1	1	1	,	L	12
1	0	1	1	1	-	M	13
0	1	1	1	1	.	N	14
1	1	1	1	1	/	O	15
0	0	0	0	0	0	P	16
1	0	0	0	0	1	Q	17
0	1	0	0	0	2	R	18
1	1	0	0	0	3	S	19
0	0	1	0	0	4	T	20
1	0	1	0	0	5	U	21
0	1	1	0	0	6	V	22
1	1	1	0	0	7	W	23
0	0	0	1	0	8	X	24
1	0	0	1	0	9	Y	25
0	1	0	1	0	:	Z	26
1	1	0	1	0	;	[	27
0	0	1	1	0	<	\	28
1	0	1	1	0	=	]	29
0	1	1	1	0	>	‾	30

* Decimal Equivilents

Figure P5-1. Talk/Listen Addresses vs. ASCII Codes

ON LINE/OFF LINE OPERATION

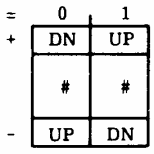
The counter may be used On Line (connected to the bus system), or Off Line (not connected to the bus). When used On Line, switches AM121S1-S7 determine the address which is assigned to the device. IMPORTANT: S7 must be in the "0" position while On Line, or erroneous operation of the counter will result. While On Line all bus operations are active; manual use of the counter as a system device is not possible.

When Off Line operation of the counter is desired, output data may be transmitted in a continuous mode by the counter if switch AM121S7 is in the "1" position when power is turned on. The counter will be initialized, and all front panel controls will be operative. In addition, S1 and S2 are in continuous control of the output sample rate (S1), and data format (S2). Figure P5-2 summarizes the operation of S1-S7, with their functional characteristics.

AM121 SWITCHES	S1	S2	S3	S4	S5	S6	S7	FUNCTION
ON LINE OPERATION	A1	A2	A3	A4	A5	x	0	Address assignment to counter. NOTE: S7 must be in 0 position.
OFF LINE OPERATION	0*	0*	x	x	x	x	1	Continuous output determined by **SAMPLE RATE** control. Exponent in scientific format.
	1*	0*	x	x	x	x	1	Continuous output - fast active. **SAMPLE RATE** control inactive. Exponent in scientific format.
	0*	1*	x	x	x	x	1	Continuous output determined by **SAMPLE RATE** control. Exponent in four output format.
	1*	1*	x	x	x	x	1	Continuous output - fast active. **SAMPLE RATE** control inactive. Exponent in four output format.
	x*	x*	x	x	x	x	0	No output.

x = Don't care. 1 = + position (see diagram). 0 = - position (see diagram).

* = May be continuously set or reset for desired results as long as S7 is in the "1" position during power up. After power up, S7 may be set to the "0" position (see diagram).

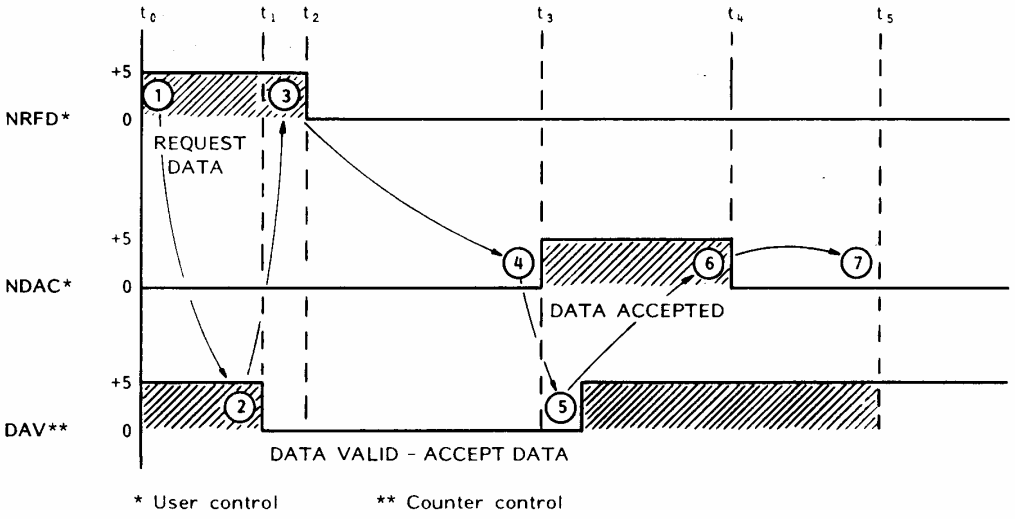


S1 - S7 SETTINGS

DN = DOWN position
UP = UP position

FIGURE P5-2. ADDRESS SWITCH ASSIGNMENTS

If the counter is used Off Line and S7 is active, ASCII data is transmitted from the counter. BCD data can easily be extracted from the ASCII data if desired. Figure P5-3 shows the timing necessary to operate the counter Off Line.



1. User requests data by taking NRFD line high.
2. Counter responds by sending DAV line low (data is now valid on DI01-DI08 and will remain so.
3. NRFD line brought low by user in response to DAV line going low (user not ready for new data).
4. NDAC line sent high, indicating user has accepted the data on the bus.
5. Counter sends DAV line high in response to NDAC high, indicating data on DI0 lines no longer valid.
6. NDAC line sent low by user in response to DAV line going high.
7. Repeat cycle from 1.

FIGURE P5-3. OFF-LINE COUNTER TIMING

Figures P5-4 and P5-5 present a sample circuit which will give the user the maximum data transfer rates in the Off Line mode. When the user sends the PRINT command high, and the data available line goes high, data is present and latched in the data latches. When the user sends the next print command, the data available line is cleared and then set when the next data byte is ready for the user. This type of data transfer is totally asynchronous, and may proceed at the users pace up to the maximum data sample rate transfer.

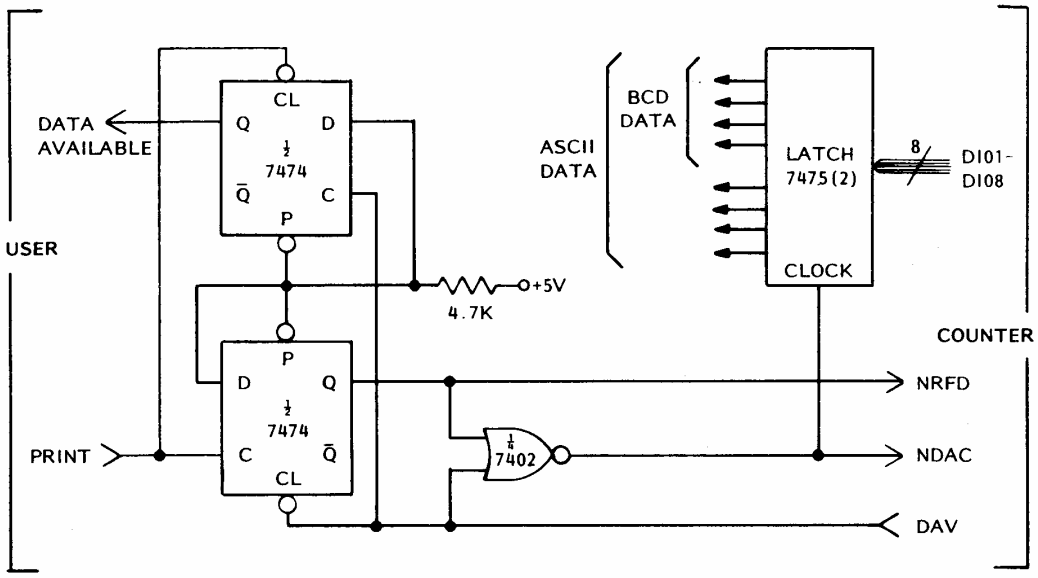


FIGURE P5-4. SAMPLE CIRCUIT OFF-LINE DATA TRANSFER

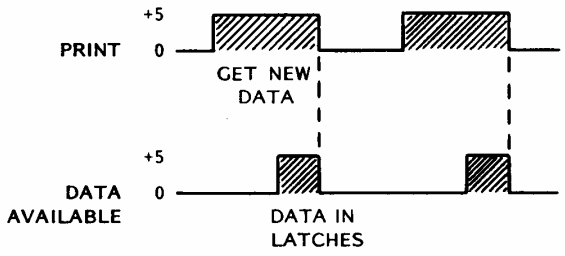


FIGURE P5-5. DATA AVAILABILITY VS. PRINT TIMING

DEVICE INDEPENDENT DATA PROGRAMMING — On Line Operation Only

Device independent data consists of the following, which is sent by the controller in charge while in the command mode:

GTL — GO TO LOCAL. This is an addressed command given by the controller — the counter must have received its LISTEN address prior to the GTL command being issued.

When GTL is received, the counter will go to the LOCAL mode with all front panel switches operative. FAST CYCLE, or the last YIG Preset command received by the counter while in the REMOTE mode, will remain and will not be cleared by this command. Front panel REMOTE indicator will be off.

SDC — SELECTED DEVICE CLEAR. An addressed command given by the controller — the counter must have received its LISTEN address prior to the SDC command being issued.

When SDC is received, the counter will be cleared to its initial state. Switches AM121 S1 thru S7 will be read.

DCL — DEVICE CLEAR. Same as SDC command except that counter's LISTEN address does not have to be received prior to issuing of DCL.

SPE — SERIAL POLL ENABLE. An addressed command given by the controller.

SPD — SERIAL POLL DISABLE.

BUS CONTROL LINES — On Line Operation Only

IFC — INTERFACE CLEAR. This command issued by the controller in charge, causes the counter to monitor the bus for instructions; all data transmission is terminated. If the counter was addressed as a listener, it will be unaddressed; if it was addressed as a talker, it will be unaddressed. Data bus (DI01-DI08) goes to the tri-state mode.

REN — REMOTE ENABLE. Issued by the controller in charge. If the counter has received its listen address while the REN line is active, the counter will go into the REMOTE mode. The programmer can now send device dependent programming data to the counter. All front panel controls except SAMPLE RATE will be inoperative.

When the REN line goes inactive, the counter will go to the LOCAL mode. YIG Preset and FAST CYCLE operation will remain at the last setting. All front panel controls will be operative.

SRQ — SERVICE REQUEST. Issued by the counter to request service from the controller. Indicates that a reading has been taken by the counter and is ready for transmission.

COUNTER ADDRESSING — On Line Operation Only

1. The counter is addressed to TALK or LISTEN by sending its assigned TALK or LISTEN address while the ATN line is active. If the counter was addressed to TALK, and the controller transmits a TALK address other than the counter's, the counter will automatically be deselected as a talker.
2. If the controller sends an UNTALK command, the counter will automatically be deselected as a talker.
3. If the counter was addressed to LISTEN, and the controller sends the counter TALK address, the counter will automatically be deselected as a listener, and be reassigned as a talker.
4. If the counter was addressed to LISTEN, and the UNLISTEN command is sent by the controller, the counter will be deselected as a listener.

POWER UP AND INITIAL CONDITIONS

After counter power has been turned on, or the commands SDC or DCL have been issued by the controller in charge, the following initial conditions exist in the counter:

1. The data bus is in the tri-state mode.
2. The counter is in the LOCAL mode.
3. The counter has sampled its address switch (S1-S7) settings.
4. The counter is not addressed to TALK or LISTEN.
5. There is no YIG Preset.
6. Transmit Normal – TN.
7. Remote – BB.
8. Remote – HP.
9. Remote – TP.
10. Remote – R4.
11. Remote – FP.
12. Remote – ES data format.
13. Remote – CA.
14. The counter and converter have been reset.

REMOTE/LOCAL OPERATION

All device dependent data is programmed into the counter while in the REMOTE mode. The REN line is set active by the controller, followed by the counter's LISTEN address, thus putting the counter in the REMOTE mode. The REMOTE indicator (on counter front panel) will light, and device commands may be programmed.

In the REMOTE mode, all front panel switches are inoperative except SAMPLE RATE. If FAST CYCLE is entered, SAMPLE RATE and HOLD also become inoperative. When switching back to the LOCAL mode ($\overline{\text{REN}}$ or GTL), all front panel switches will be active, and the programmed information which was present while in the REMOTE mode, will still be present if the counter returns to the REMOTE mode. Fast active, or YIG Presets, are active in both LOCAL or REMOTE modes, but can be programmed only during REMOTE operations.

DEVICE DEPENDENT DATA PROGRAMMING – On Line Operation Only

Device dependent data is that data, inputted in string form, to which the counter uniquely responds while in the REMOTE mode, and while addressed to LISTEN.

While in the command mode, the controller places the counter in the REMOTE mode by setting the REN line active, then by sending the listen address of the counter. When the counter is in the REMOTE mode and addressed to LISTEN, the controller leaves the command mode and enters the date transfer mode. It is in this mode and counter set-up, that device dependent data can be sent by the programmer. The following list shows mnemonics, format, and specifications, for the device dependent data.

GENERAL FORMAT

MNEMONIC – Two alpha characters, or one alpha and one numeric character, depending upon the function being programmed.

SIGN – The sign "+" or "-" of the value portion of the function being programmed. (The "+" sign is optional.

VALUE – The particular numeric value assigned to the function being programmed. Leading and trailing zeros need not be programmed.

SCALE FACTOR – Exponent symbol used with the value portion of the function being programmed. "M" = megahertz (10^6), G = Gigahertz (10^9).

NOTE: If any of the above does not pertain to the particular function being programmed, it should be omitted.

EXAMPLE: BA. BA is the MNEMONIC. The SIGN, VALUE, and SCALE FACTOR are not necessary. This function sets the counter to Band A.

YIG PRESET

This command will program a YIG Preset equal to the VALUE and SCALE FACTOR. Negative YIG Presets will be taken as positive. MNEMONIC: YP, SIGN: +(optional), VALUE and SCALE FACTOR.

EXAMPLE: YP M YP 1.2 G or YP M YP - 1.2 G: Both program 1.2×10^9 Hz (1.2 GHz) into the counter.

EXAMPLE: YP M or YP G: Clears the YIG Preset.

NOTE: Before issuing any new preset numbers, use the YP M command to clear the register.

YIG PRESET RANGE: Refer to Section 3.

Between YP and M or G, only the sign, numeric values, or decimal point, will be recognized by the counter.

NOTE: In the following commands, the MNEMONIC code is shown following the command title. SIGN, VALUE, and SCALE FACTOR are not used.

RESET COUNTER AND CONVERTER (RC): This command resets both the basic counter and converter portions of the 451, and causes the counter to take a new reading. When RC is sent, a reset occurs; to obtain another reset, RC must be resent.

HOLD ACTIVE (HA): When HA is sent in the REMOTE mode, the counter stops taking readings, data transmission is stopped, and the last frequency read is displayed and held by the counter. In the FAST ACTIVE mode (see FA command), the HA command will have no effect upon the counter's display operation while in the LOCAL mode, but will stop data transmission. If programmed during the FA mode, and FA is then terminated, the counter will respond to the HA command.

HOLD PASSIVE (HP): This command terminates HA.

1 MS GATE ACTIVE (TA): This command puts the counter in the 1 ms gate time mode.

1 MS GATE PASSIVE (TP): This command terminates TA.

BAND A (BA): This command selects Band A (Option P2) of the counter – 300 MHz to 950 MHz.

BAND B (BB): This command selects Band B of the counter – 925 MHz to 18 GHz.

CONVERTER AUTO (CA): This command selects the AUTO SWEEP mode of the counter, and operates in conjunction with the YIG Preset (YP) command and value.

CONVERTER MANUAL (CM): This command selects the MANUAL SELECT mode of the counter, and operates in conjunction with YIG Preset (YP) command and value.

TRANSMIT NORMAL (TN): This command causes the counter to continuously transmit its reading when addressed to talk.

TRANSMIT SERVICE REQUEST (TS): This command causes the counter to take a reading, format the data, store the result, and activate the SRQ line to indicate to the controller that a reading is ready for transmission. After the reading is transmitted, the SRQ line is deactivated and the process is repeated. The status byte transmitted during serial polling indicates that data is ready for transmission (bit 7 active).

NOTE: REMOTE RESOLUTION commands determine the resolution of the counter readings while in the REMOTE mode.

REMOTE RESOLUTION (R4): Resolution of 10 kHz.

REMOTE RESOLUTION (R5): Resolution of 100 kHz.

REMOTE RESOLUTION (R6): Resolution of 1 MHz.

FAST ACTIVE (FA): The FA command causes the counter to go into the fast cycle mode of operation. In this mode, the front panel SAMPLE RATE/HOLD control is inactive, and the fastest sample rate transmissions are attained.

FAST PASSIVE (FP): This command terminates FA.

EXPONENT – SCIENTIFIC OUTPUT (ES): This command causes the counter to output data in an engineering notation format (see Output Data Format) if counter is addressed to TALK.

EXPONENT – FOUR OUTPUT (E4): This command causes the counter to provide data in four exponent format (see Output Date Format) if counter is addressed to TALK.

OUTPUT DATA FORMAT

The output data is transmitted with the most significant byte first, in a bit-parallel, byte-serial form, and in 7-bit ASCII code. The general format is:

xx.xxx xx E y CR LF

where *CR* is Carriage Return, *LF* is Line Feed, *x* represents digits 1 through 9, and *y* the exponent 0, 3, 6, or 9. The decimal point will be located in the proper place, though it may be deleted depending on the data output format and/or the reading.

There will always be 12 bytes of information transmitted per reading. Leading zeros are always replaced with ASCII code NULL characters. The last four bytes transmitted are always:

E y CR LF

where *y* represents exponents 0, 3, 6, or 9, and *CR* and *LF* the ASCII codes used as delineators.

The ASCII code character *E* is used to specify the exponent 0, 3, 6, or 9, depending upon the value and format of the reading. Thus the data output command ES affects only the numeric portion and exponent value of the transmitted data.

The maximum frequency that can be transmitted is: 99.99999 GHz.

EXPONENT – FOUR OUTPUT (E4) FORMAT

In the E4 format, the exponent value of the transmitted data will always be four (4) with no decimal point inserted. The reading will be transmitted as seen on the counter's front panel display, with the resolution of the reading dependent upon the front panel switches or the remote resolution commands. The digits affected by the resolution setting are set to zero. Some examples in the E4 format are as follows, with *N* representing an ASCII NULL character.

Reading on display: 11 234.56 MHz

RESOLUTION	READING TRANSMITTED
10 kHz	N1123456 E4 CR LF
100 kHz	N1123450 E4 CR LF
1 MHz	N1123400 E4 CR LF

Reading on display: 434.56 MHz

RESOLUTION	READING TRANSMITTED
10 kHz	NNN43456 E4 CR LF
100 kHz	NNN43450 E4 CR LF
1 MHz	NNN43400 E4 CR LF

EXPONENT – SCIENTIFIC OUTPUT (ES) FORMAT

In the ES format, the exponent value of the transmitted data is always 0, 3, 6, or 9, depending on the frequency reading. A decimal point is entered to correspond to the exponent so the transmitted data will be a mixed number of whole and fractional parts. Example: 345.727, 45.72, 5.2, etc.

All leading zeros are transmitted as ASCII NULL characters, and the digits which are affected by the remote resolution are disregarded. (NULL characters are inserted at the beginning of the data so 12 characters are always transmitted.)

If the resolution or frequency reading includes a decimal point that is not necessary, the decimal point is disregarded and a NULL character is inserted at the beginning of the data.

If the resolution affects the whole part of the number being transmitted (no decimal point or fractional part), zeros are inserted for those numbers before being transmitted.

If the resolution covers the entire number, then all NULLS are transmitted with the exponent value of the reading, so the user can tell by the exponent value just how the resolution covered the reading. For example: 0 Hz is transmitted as: NNNNNNN0E0 CR LF.

When local resolution is used (by pressing the RESOLUTION switches on the counter front panel), those digits affected by the resolution are replaced by zeros. Examples in the ES format are:

Frequency input: 1 234.56 MHz

REMOTE RESOLUTION	READING TRANSMITTED
10 kHz	N 1.23456 E9 CR LF
100 kHz	NN 1.2345 E9 CR LF
1 MHz	NNN 1.234 E9 CR LF

Frequency input: .56 MHz

REMOTE RESOLUTION	READING TRANSMITTED
10 kHz	NNNNN E3 CR LF
1 GHz	NNNNNNNN E3 CR LF

Output frequency transmissions as shown on a printer. NOTE: Leading NULL characters are not printed.

PRINTER OUTPUT	FREQUENCY
34.6E6	34 600 000 Hz
21.7693E9	21 769 300 000 Hz
39.99999E9	39 999 99 0000 Hz
0E0	0 Hz
E6	? but in MHz range

PROGRAMMING EXAMPLE USING HP 9815 CALCULATOR AS A CONTROLLER

The program shown in Figure P5-6 sets the counter as follows:

a. Band A (BA)
b. Remote Resolution - 10 kHz (R4)
c. 1 ms Gate Passive (TP)
d. Hold Passive (HP)
e. Fast Active (FA)
f. Exponent Scientific (ES)
g. No YIG Preset (YPM)

The program then takes a frequency reading and makes a print out. Input frequency is 480.75xxxx MHz, where *x* is the frequency variation.

EXAMPLE:
480750000
480750000
480760000
480750000
480750000
480760000
480750000
480750000
480750000
480750000
480750000

The character *E* and exponent values are not presented; however, this is entirely dependent on the controller. Although the information was sent, the controller formatted and printed the data in this form. The way in which output data may be interpreted, and how data is sent to the counter is entirely dependent on the controller used.

Programs may be written to display the entire data transmission. The program sampled the frequency at different resolutions and printed the results.

EXAMPLE:

```
RESOLUTION SCAN
.................
       285.24E6
        285.1E6
          285E6
        285.2E6
       285.06E6
.................
   OFFSET SHIFT
.................
           0E0
         900E3
         9.9E6
        99.9E6
       999.9E6
     9.9999E9
```

Figure P5-7 summarizes the counter commands which are available with this option.

PROGRAM STEP	COMMAND	COMMENT
0000	Clear	Clear counter
0001	CMD 5	Controller to COMMAND mode
0003	@	
0004	B	Set REN line active
0005	END	Clear COMMAND mode
0006	CMD 5	Enter COMMAND mode
0008	U	Controller talk address
0009	.	
0010	3	Counter listen address
0011	Blank	Counter goes to data transfer mode
0012	B	Device dependent data starts here.
0013	A	Counter set to Band A
0014	R	Resolution 4
0015	4	"
0016	T	1 ms Gate Passive
0017	P	"
0018	H	Hold Passive
0019	P	"
0020	F	Fast Active
0021	A	"
0022	E	Exponent - Scientific
0023	S	"
0024	Y	Clear YIG Preset
0025	P	"
0026	M	"
0027	END	End device dependent mode
0028	Clear	
0029	1	
0030	Enter	
0031	1	
0032	9	
0033	Read 5	Read frequency
0034	Print	
0035	Go to 0028	Repeat
0036	END	

FIGURE P5-6. TYPICAL PROGRAM

FUNCTION	ASCII	MNEMONIC	SIGN	VALUE	COMMENTS
YIG Preset		YP	+	YIG Preset range	+ sign optional
Reset Counter and Conv.		RC			One-shot action
Converter Auto		CA			
Converter Manual		CM			
Hold Active		HA			No data transmsn.
Hold Passive		HP			
1 ms Gate Time Active		TA			Gate time: 1 ms
1 ms Gate Time Passive		TP			Gate time: 100 μs
Band A		BA			
Band B		BB			
Remote Resolution: 10 kHz		R4			
Remote Resolution: 100 kHz		R5			
Remote Resolution: 1 MHz		R6			
Fast Active		FA			Sample rate
Fast Passive		FP			Sample rate
Transmit Normal		TN			
Transmit Service Request		TS			
Exponent - Scientific		ES			Output Data
Exponent - Four		E4			Output Data
Device Clear (DCL)	DC4				Contlr. Dpndnt.
Selected Device Clear SDC)	EOT				Contlr. Dpndnt.
Go to Local Control (GTL)	SOH				Contlr. Dpndnt.
Serial Poll Enable (SPE)	CAN				Contlr. Dpndnt.
Serial Poll Disable (SPD)	EM				Contlr. Dpndnt.
My Listen Address (MLA)					Device Dpndnt.
My Talk Address (MTA)					Device Dpndnt.
Unlisten	?				Contlr. Dpndnt.
Untalk	—				Contlr. Dpndnt.

FIGURE P5-7. PROGRAMMING SUMMARY CHART

AM100
GPIB MICROPROCESSOR
(2020060)

The microprocessor PC board (AM100) provides control of BCD board AM120. Remote/Local board AM121, the interface bus, and associated counter functions.

CIRCUIT DESCRIPTION

CLOCK CIRCUIT: Timing for the microprocessor and associated logic is generated through clock chip U2. An external 5.185 MHz crystal is used to generate a two-phase 740 kHz clock ($\emptyset 1$, $\emptyset 2$). In addition to clock generation, U2 also provides a power up reset pulse. This pulse is produced by timing circuit R1/C1.

CENTRAL PROCESSING UNIT (CPU): All GPIB and counter interface functions are controlled by microprocessor U1. The cycle time of the CPU (10.8 μs) is divided into eight sections. During the first three time sections (A1, A2, A3), the address is sent through the data bus (D_0 - D_3) and latched in the ROM's. During the next two time sections (M1, M2), an instruction is sent from the ROM addressed and latched into U1 (the instruction is also on D_0 - D_3). During the last three time sections, the instruction received by U1 is executed, and the data bus (D_0 - D_3) is used by U1 to transfer data to the RAM or I/O ports. At the beginning of each cycle, a sync pulse is generated by U1 which is sent to all the I/O and memory elements associated with the processor, and to buffer U9. U9 output is used by the BCD board to generate timing pulses.

The CPU also generates the proper I/O and RAM bank select lines (CM-RAM_{0_3}) during the execution portion of the processor cycle. The test input to U1 comes from the rear panel address switches (AM121S1-S5), and corresponds to switch A5. When power is turned on, the reset pulse from U2 causes the program counter in the CPU to be reset to 000 (HEX), and the processor to start obtaining instructions from that location in the ROM.

1K x 8 ROM: U7 is a 1K x 8 ROM which holds the first 1K of the 2K system program. In addition, U7 contains twelve I/O ports which supply the 3MSD + OFFSET outputs to the counter through connector J1. The ATN RESET signal to U18 comes from an I/O line on the ROM.

This control signal resets the ATN F/F after an attention call from the interface bus has been received. Pull down resistor network RN1 is used to make these outputs TTL compatible.

20 x 4 x 4 RAM: U4 is a random access memory organized into four groups of twenty 4-bit bytes. In addition to being used as storage for status and intermediate information, the RAM utilizes two of its four I/O lines. These I/O lines (designated SR CLK and SR DATA) transmit the YIG Preset information received over the GPIB to the shift register located on BCD board AM120). U8 is used as a buffer for the I/O lines.

I/O PORTS: Three I/O port IC's (U3, U5, U6) supply information to the counter and internal logic. U3 receives the following input data from the GPIB: $\overline{ID1}$ to $\overline{ID7}$, REN (Remote Enable line), IIFC (Interface Clear), IDAV (Data Available). The output signals to the GPIB are: ORFD (Ready For Data), and ODAC (Data Accept). In addition, the input lines $\overline{Remote}$/Local Select lets the processor know if the counter is in the remote or local mode, and ATN $\overline{FLAG}$ lets the counter know if the Attention F/F (U18) has been set. Output lines Prog. $\overline{Reset}$, resets the counter during power up, and 3MSD FLAG $\overline{Reset}$ controls 3MSD Flag Logic IC's U10 and U11 (both are used for internal logic control).

I/O port U5 controls the first half of the output data to the GPIB: $\overline{OD1}$ - $\overline{OD4}$, and $\overline{ODAV}$ (Data Available line). The BCD inputs from BCD board AM120: BCD A through BCD D, are inputs to this port. The $\overline{Listen}$/Talk output controls GPIB driver MUX U17, and places drivers U13 and U14 in the high impedance state when in the Listen mode, and turns on U13 and U14 when in the Talk mode. The FAST signal from U5 controls the cycle time of the counter, and when active, puts the counter in the Fast Cycle mode.

I/O port U6 receives the 3MSD number from the counter. In addition, the second half of the output data ($\overline{OD5}$-$\overline{OD7}$) is transmitted to the GPIB. The signal μP INH, is used by the processor to stop the counter in the Print Sequence.

GPIB DRIVERS/RECEIVERS: The Drivers/Receivers which interface with the GPIB are U13-U16. These signals go to J2 and J6, and interface to the GPIB standard connector on AM120.

GPIC CONTROL: GPIB control logic consists of U12, U17-U18. U18 includes the ATN and IFC latches used to latch the control line signals from the GPIB for later use by the processor. U17 is the MUX which controls the drivers for proper response to an ATN Active, or IFC Active signal from the GPIB.

-10 V REGULATOR: U19, Q1, and Q2 comprise the regulator which drops the -12 V of the counter power supply to the -10 V required by the processor system.

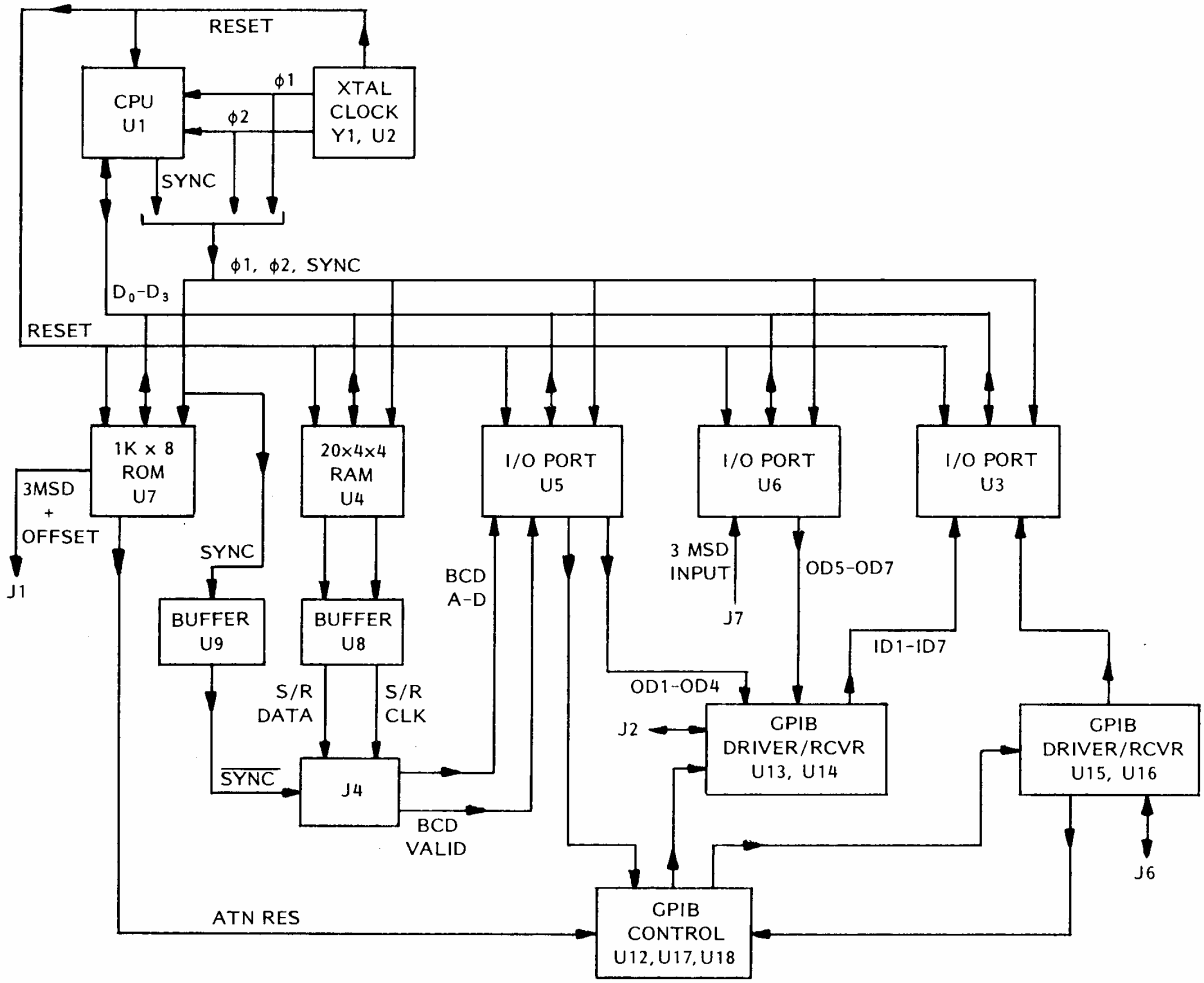


FIGURE P5-8. GPIB MICROPROCESSOR DIAGRAM

AM 100 MICROPROCESSOR, GPIB

2020060 - K

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
AM100	Microprocessor, GPIB	2020060	1		34257
C1	Tant, 1.0μF, , 35V	2300008	2	TAG20 - 1.0/35-50	14433
C2	Mica, 30pF, 5%, 500V	2250024	2	DM15-300J	72136
C3	C2				
C4	Cer, .1μF, 20%, 16V	2150012	2	RT-16-0.1Z	0000R
C5	Cer, .01μF, 20%, 100V	2150003	8	TG - S10	56289
C6	C5				
C7	C4				
C8	C1				
C9	Tant, 10μF, 20%, 25V	2300029	2		
C10	C9				
C11	Tant, 33μF, 20%, 20V	2300023	1	TAG20 - 33/20	14433
C12 thru C17	C5				
CR1	General Purpose	2704154	1	IN4154	07263
Q1	PNP, General Purpose	4704126	1	2N4126	04713
Q2	PNP, Power	4710002	1	MJE370	04713
R1	Comp, 1M, 5%, 1/4 W	4010105	1	RC07GF105J	81349
R2	Comp, 1K, 5%, 1/4 W	4010102	1	RC07GF102J	81349
R3	Comp, 10K, 5%, 1/4 W	4010103	1	RC07GF103J	81349
R4	Comp, 12K, 5%, 1/4 W	4010123	6	RC07GF123J	81349
R5 thru R9	R4				
R10	Comp, 24K, 5%, 1/4 W	4010243	1	RC07GF243J	81349
R11	Comp, 4.7K, 5%, 1/4 W	4010472	1	RC07GF472J	81349
R12	Met Ox, 24K, 2%, 1/4 W	4130243	1	C4/2%/243	24546
R13	Met Ox, 20K, 2%, 1/4 W	4130203	1	C4/2%/203	24546
R14	Comp, 100, 5%, 1/8 W	4010101	2	RC07GF101J	81349
R15	R14				
RN1	Resistor Network, 15K, 2%, 1/8 W	4170001	1	898-1-R15K	80740
U1	4 Bit CPU	3054040	1	C4040	34649
U2	Clock Generator	3054201	1	P4201	34549
U3	PGRM, General Purpose RAM	3054265	3	P4265	34649
U4	320 Bit RAM	3054002	1	P4002-1	34649
U5	U3				
U6	U3				
U7	1024X8Bit ROM	3150003	1	4308/315-03	34649
U8	High Speed Hex Inverter	3050005	1	8T93A	18324

AM 100 MICROPROCESSOR, GPIB

2020060 - K

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U9	Voltage Comparator	3050311	1	LM311N	0000X
U10	Quad, 2IN, NAND Gate	3007400	1	DM7400	0000X
U11	Not Used				
U12	Quad, 2 INP, NOR Gate	3087402	1	74LS02P	01295
U13	Quad, GPIB Transcor	3013441	3	MC3441P	04713
U14	U13				
U15	U13				
U16	Quad, GPIB, Transcor	3013440	1	MC3440P	04713
U17	Quad, 2:1 MUX, Inv. Out	3070008	1	74S158P	01295
U18	Dual D Flip-flop	3087474	1	DM74LS74P	01295
U19	Op Amplifier	3040741	1	LM741CN	0000X
Y1	Crystal, 5.185 MHz	2030013	1	CY8A, EIP	34257

PAGE LEFT BLANK INTENTIONALLY

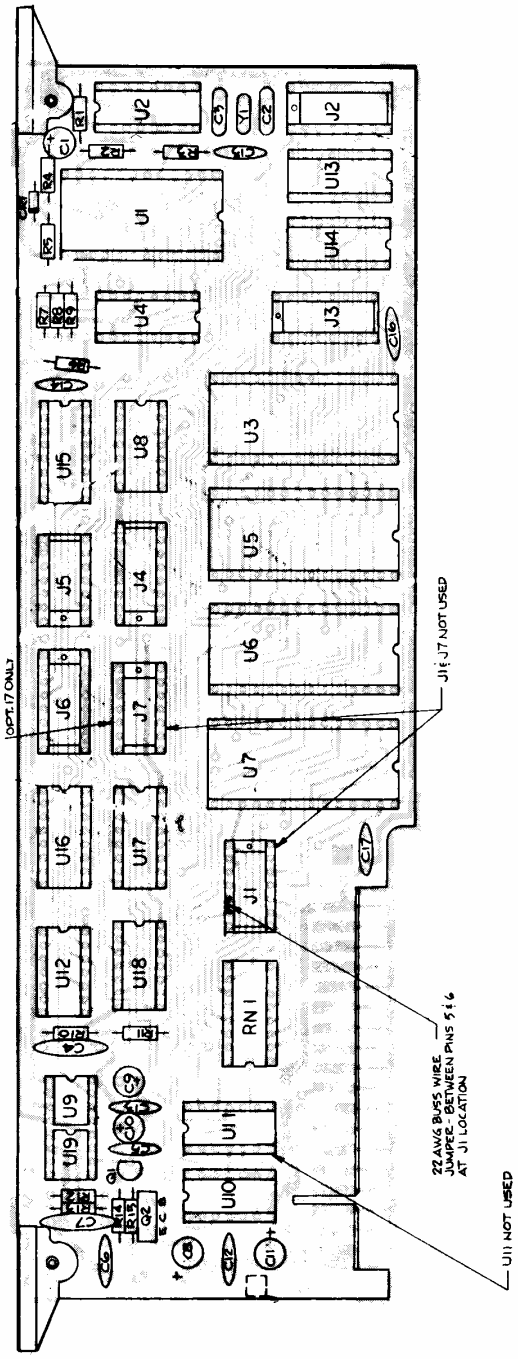


Figure P5-9. GPIB Microprocessor Component Locator

AM100
GPIB MICROPROCESSOR
(2020213

The microprocessor PC board (AM100) provides control of BCD board AM120. Remote/Local board AM121, the interface bus, and associated counter functions.

CIRCUIT DESCRIPTION

CLOCK CIRCUIT: Timing for the microprocessor and associated logic is generated through clock chip U2. An external, 5.185 MHz crystal is used to generate a two-phase 740 kHz clock (Ø1, Ø2). In addition to clock generation, U2 also provides a power up reset pulse. This pulse is produced by timing circuit R1/C1.

CENTRAL PROCESSING UNIT (CPU): All GPIB and counter interface functions are controlled by microprocessor U1. The cycle time of the CPU (10.8 μs) is divided into eight sections. During the first three time sections (A1, A2, A3), the address is sent through the data bus (D_0 - D_3) and latched in the ROM's. During the next two time sections (M1, M2), an instruction is sent from the ROM addressed and latched into U1 (the instruction is also on D_0 - D_3). During the last three time sections, the instruction received by U1 is executed, and the data bus (D_0 - D_3) is used by U1 to transfer data to the RAM or I/O ports. At the beginning of each cycle, a sync pulse is generated by U1 which is sent to all the I/O and memory elements associated with the processor, and to buffer U9. U9 output is used by the BCD board to generate timing pulses.

The CPU also generates the proper I/O and RAM bank select lines (CM - RAM_{0-3}) during the execution portion of the processor cycle. The test input to U1 comes from the rear panel address switches (AM121S1-S5), and corresponds to switch A5. When power is turned on, the reset pulse from U2 causes the program counter in the CPU to be reset to 000 (HEX), and the processor to start obtaining instructions from that location in the ROM.

1K x 8 ROM: U7 is a 1K x 8 ROM which holds the first 1K of the 2K system program. In addition, U7 contains twelve I/O ports which supply the 3MSD + OFFSET outputs to the counter through connector J1. The ATN RESET signal to U18 comes from an I/O line on the ROM.

This control signal resets the ATN F/F after an attention call from the interface bus has been received. Pull down resistor network RN1 is used to make these outputs TTL compatible.

20 x 4 x 4 RAM: U4 is a random access memory organized into four groups of twenty 4-bit bytes. In addition to being used as storage for status and intermediate information, the RAM utilizes two of its four I/O lines. These I/O lines (designated SR CLK and SR DATA) transmit the YIG Preset information received over the GPIB to the shift register located on BCD board AM120). U8 is used as a buffer for the I/O lines.

I/O PORTS: Three I/O port IC's (U3, U5, U6) supply information to the counter and internal logic. U3 receives the following input data from the GPIB: $\overline{ID1}$ to $\overline{ID7}$, REN (Remote Enable line), IIFC (Interface Clear), IDAV (Data Available). The output signals to the GPIB are: ORFD (Ready For Data), and ODAC (Data Accept). In addition, the input lines $\overline{Remote}$/Local Select lets the processor know if the counter is in the remote or local mode, and ATN $\overline{FLAG}$ lets the counter know if the Attention F/F (U18) has been set. Output lines Prog. $\overline{Reset}$, resets the counter during power up. U11 and U20 provide a timeout signal which brings ORFD and ODAC low for 5 ms while the counter exits the handshake process. U21 and U20 are used to latch the ORFD line and provide the proper timing between ORFD and ODAC.

I/O port U5 controls the first half of the output data to the GPIB: $\overline{OD1}$ - $\overline{OD4}$, and $\overline{ODAV}$ (Data Available line). The BCD inputs from BCD board AM120: BCD A through BCD D, are inputs to this port. The $\overline{Listen}$/Talk output controls GPIB driver MUX U17, and places drivers U13 and U14 in the high impedance state when in the Listen mode, and turns on U13 and U14 when in the Talk mode. The FAST signal from U5 controls the cycle time of the counter, and when active, puts the counter in the Fast Cycle mode.

I/O port U6 receives the 3MSD number from the counter. In addition, the second half of the output data ($\overline{OD5}$-$\overline{OD7}$) is transmitted to the GPIB. The signal μP INH, is used by the processor to stop the counter in the Print Sequence.

GPIB DRIVERS/RECEIVERS: The Drivers/Receivers which interface with the GPIB are U13-U16. These signals go to J2 and J6, and interface to the GPIB standard connector on AM120.

GPIC CONTROL: GPIB control logic consists of U12, U17-U18. U18 includes the ATN and IFC latches used to latch the control line signals from the GPIB for later use by the processor. U17 is the MUX which controls the drivers for proper response to an ATN Active, or IFC Active signal from the GPIB.

-10 V REGULATOR: U19, Q1, and Q2 comprise the regulator which drops the -12 V of the counter power supply to the -10 V required by the processor system.

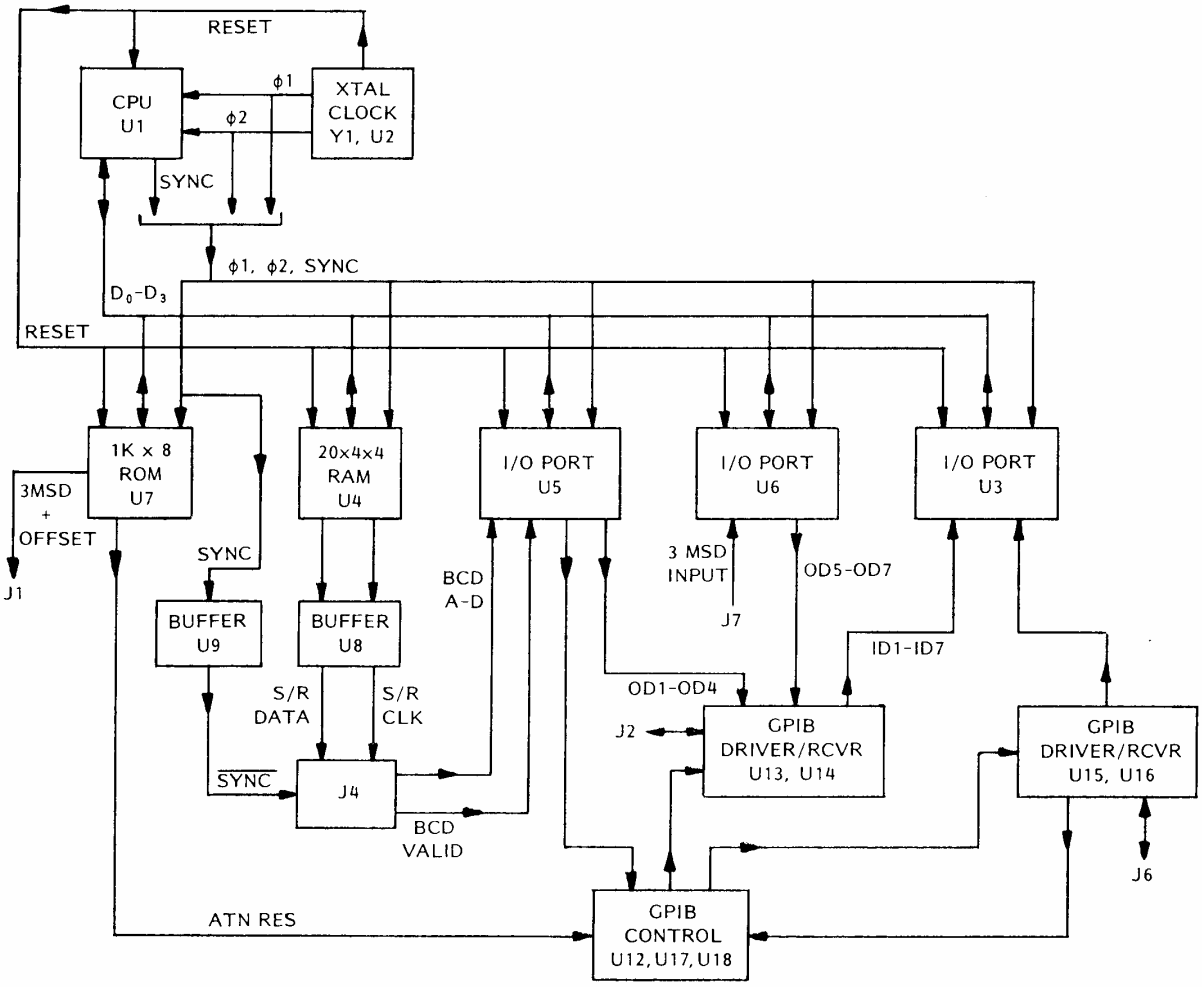


FIGURE P5-8. GPIB MICROPROCESSOR DIAGRAM

AM 100 MICROPROCESSOR, GPIB

2020213-01 - B

REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
AM100	Microprocessor, GPIB	2020213-01	1	EIP	34257
C1	Tant, 1.0μF, 20%, 35V	2300008-00	2	TAG20 - 1.0/35-50	14433
C2	Mica, 30pF, 5%, 500V	22500024-00	2	DM15-300J	72136
C3	C2				
C4	Cer,. 1μF, 20%, 16V	2150012-00	5	RT-16-0.1Z	0000R
C5	Cer, .01μF, 20%, 100V	2150003-00	8	TG-S10	56289
C6	C5				
C7	C4				
C8	C1				
C9	Tant, 10μF, 20%, 25V	2300029-00	2	DF106M25S	72136
C10	C9				
C11	Tant, 33μF, 20%, 20V	2300023-00	1	TAG20 - 33/20	14433
C12 thru C17	C5				
C18 thru C20	C4				
CR1	General Purpose	2704154-00	2	IN4154	07263
CR2	CR1				
Q1	PNP, General Purpose	4704126-00	1	2N4126	04713
Q2	PNP, Power	4710002-00	1	MJE370	04713
R1	Comp, 1M, 5%, 1/4 W	4010105-00	1	RC07GF105J	81349
R2	Comp, 1K, 5%, 1/4 W	4010102-00	1	RC07GF102J	81349
R3	Comp, 10K, 5%, 1/4 W	4010103-00	2	RC07GF103J	81349
R4	Comp, 12K, 5%, 1/4 W	4010123-00	6	RC07GF123J	81349
R5 thru R9	R4				
R10	Comp, 24K, 5%, 1/4 W	4010243-00	1	RC07GF243J	81349
R11	Comp, 4.7K, 5%, 1/4 W	4010472-00	1	RC07GF472J	81349
R12	Met Ox, 24K, 2%, 1/4 W	4130243-00	1	C4/2%/243	24546
R13	Met Ox, 20K, 2%, 1/4 W	4130203-00	1	C4/2%/203	24546
R14	Comp, 100, 5%, 1/8 W	4010101-00	2	RC07GF101J	81349
R15	R14				
R16	R3				
R17	Comp, 56K, 5%, 1/4 W	4010563-00	1	RC07GF563J	81349
R18	Comp, 100, 5%, 1/4 W	4010104-00	1	RC07GF104J	81349
R19	Comp, 15K, 5%, 1/4 W	4010153-00	1	RC07GF153J	81349

AM 100 MICROPROCESSOR, GPIB, continued

2020213-01 - B

REF DES	DESCRIPTION	EIP NO.	PER ASSY	TYP MFG NO.	TYP FSCM NO.
U1	4 Bit CPU	3054040-00	1	C4040	34649
U2	Clock Generator	3054201-00	1	P4201	34549
U3	PGRM, General Purpose RAM	3054265-00	3	P4265	34649
U4	320 Bit RAM	3054002-00	1	P4002-1	34649
U5	U3				
U6	U3				
U7	1024X8Bit ROM	3150003-00	1	4308/315-03	34649
U8	High Speed Hex Inverter	3050005-00	1	8T93A	18324
U9	Voltage Comparator	3050311-00	1	LM311N	0000X
U10	Quad, 2IN, NAND Gate	3007400-00	2	DM7400	0000X
U11	One Shot	3084123-00	1	DM74LS123	0000X
U12	Quad, 2 INP, NOR Gate	3087402-00	1	74LS02P	01295
U13	Quad, GPIB Transcor	3013441-00	3	MC3441P	04713
U14	U13				
U15	U13				
U16	Quad, GPIB, Transcever	3013440-00	1	MC03440P	04713
U17	Quad, 2:1 MUX, Inv. Out	3070008-00	1	74S158P	01295
U18	Dual D Flip-flop	3087474-00	2	DM74LS74P	01295
U19	Op Amplifier	3040741-00	1	LM741CN	0000X
U20	U10				
U21	U18				
Y1	Crystal, 5.185 MHz	2030013-00	1	CY8A, EIP	34257

PAGE LEFT BLANK INTENTIONALLY

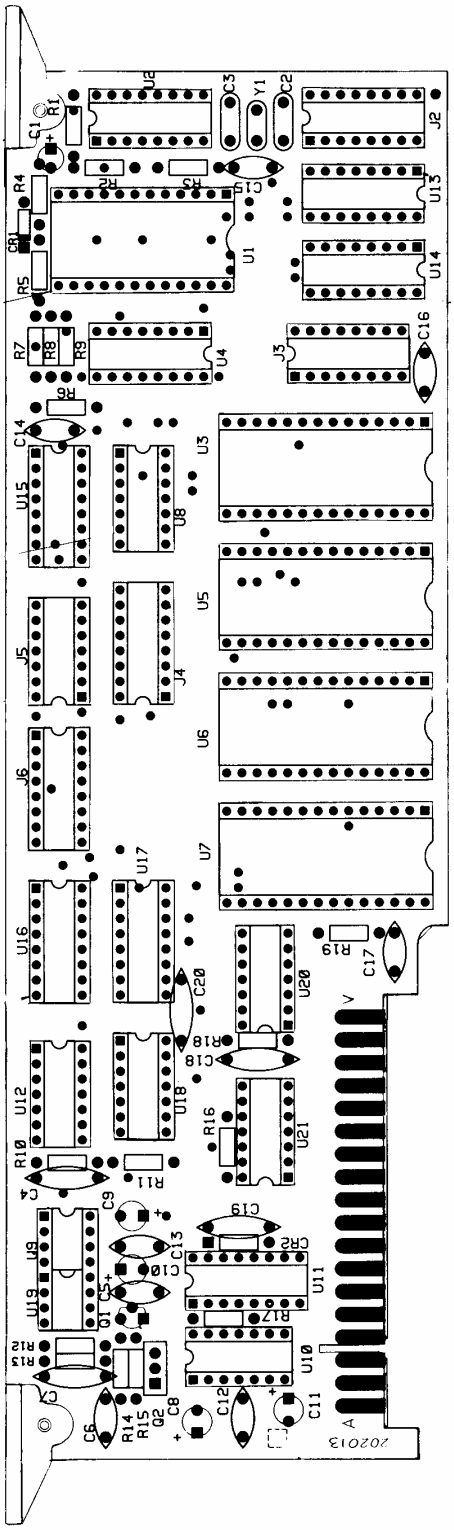
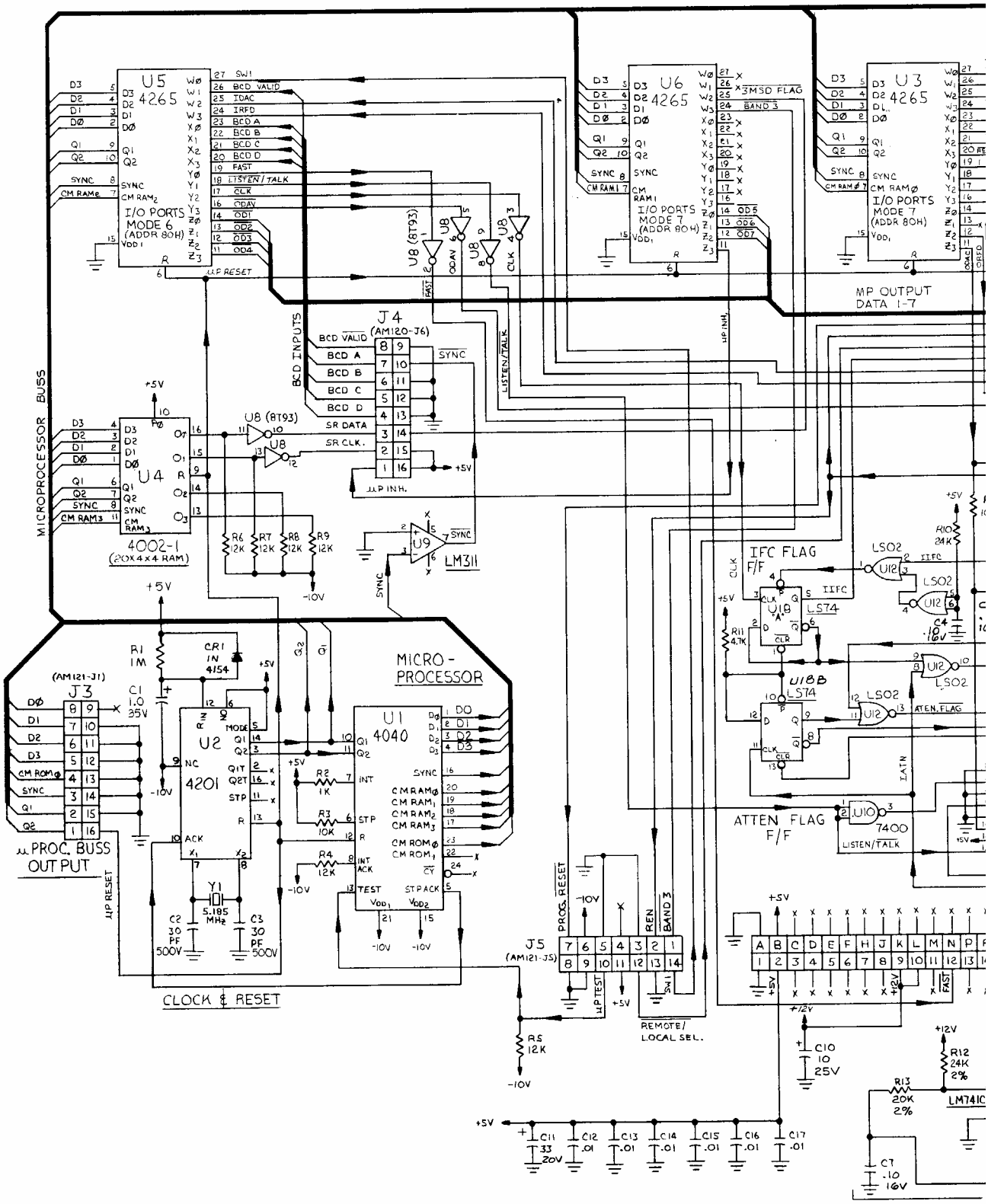
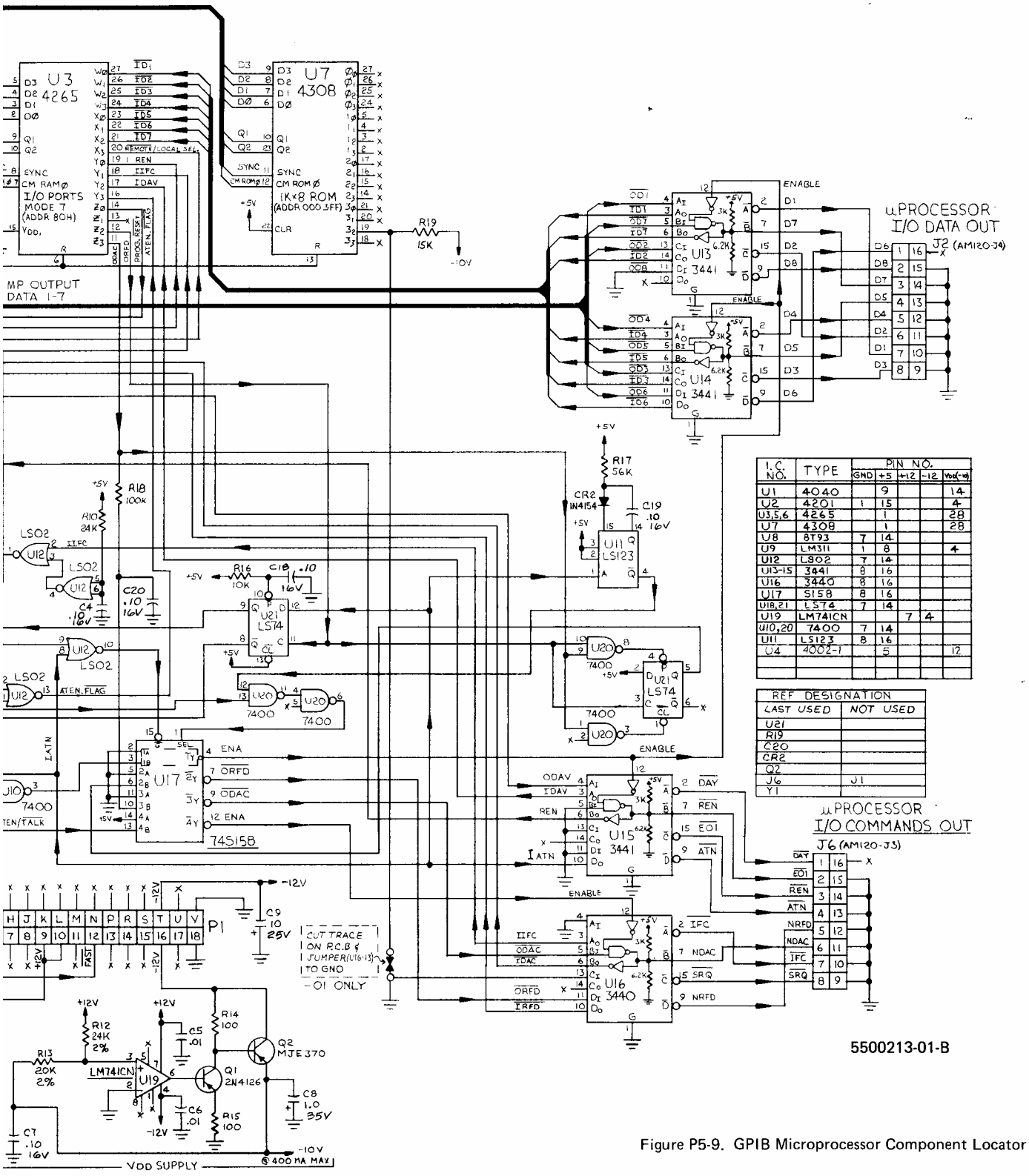


Figure P5-9. GPIB Microprocessor Component Locator

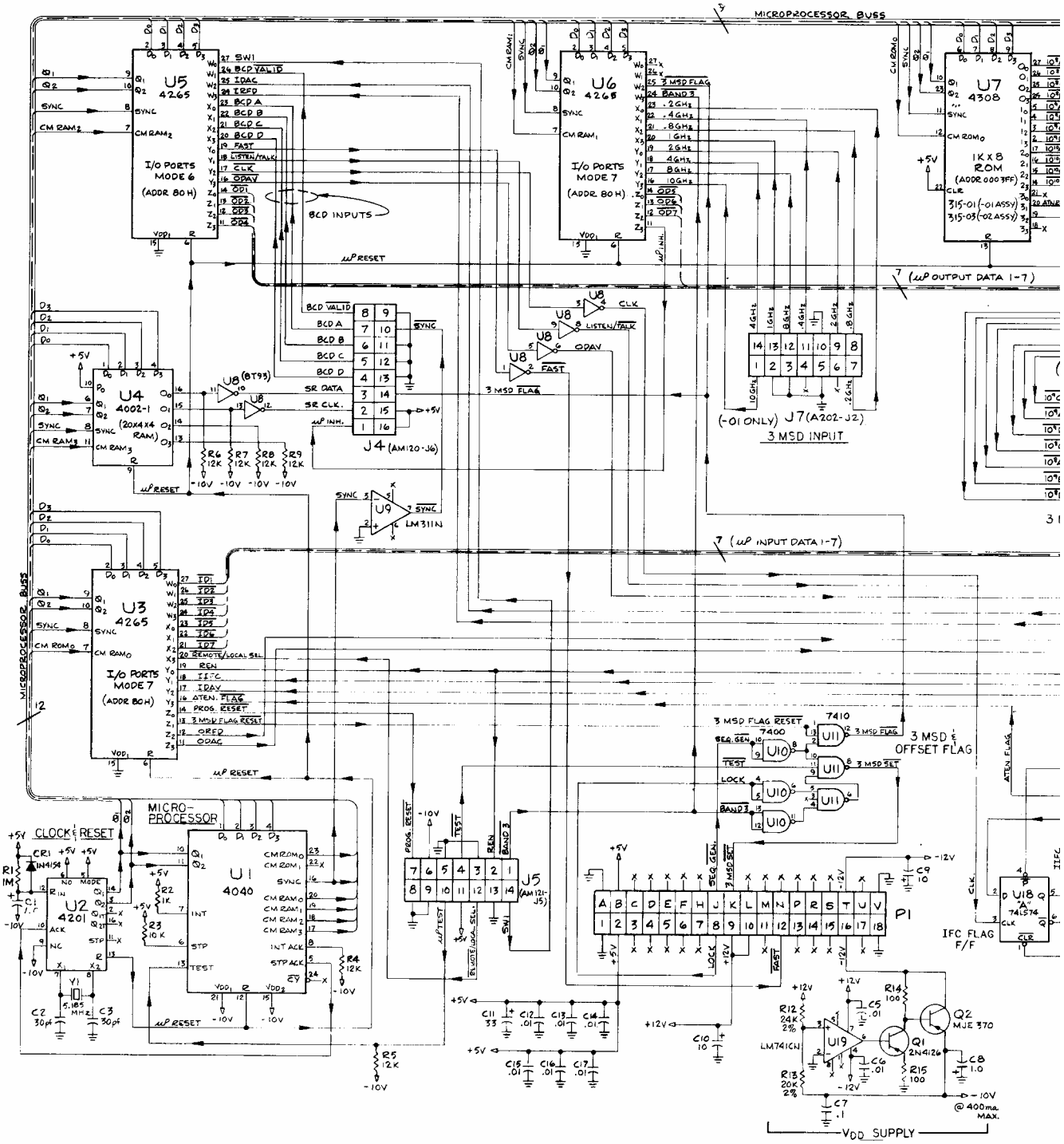

U5
4265
I/O PORTS
MODE 6
(ADDR 80H)
U6
4265
I/O PORTS
MODE 7
(ADDR 80H)
U3
4265
I/O PORTS
MODE 7
CM RAMØ
U4
4002-1
(20X4X4 RAM)
U1
4040
MICRO-
PROCESSOR
U2
4201
J3
(AM121-J1)
J4
(AM120-J6)
J5
(AM121-J5)
MICROPROCESSOR BUSS
BCD INPUTS
BCD VALID
BCD A
BCD B
BCD C
BCD D
SR DATA
SR CLK.
SYNC
LISTEN/TALK
FAST
MP OUTPUT
DATA 1-7
IFC FLAG
F/F
ATTEN FLAG
F/F
ATEN.FLAG
PROG. RESET
REMOTE/
LOCAL SEL.
CLOCK & RESET
LM311
LM741C
7400
LS02
LS74
U8 (8T93)
+5V
-10V
+12V
5.185
MHz
R1 1M
C1 1.0 35V
C2 30 PF 500V
C3 30 PF 500V
R2 1K
R3 10K
R4 12K
R5 12K
R6 12K
R7 12K
R8 12K
R9 12K
R10 24K
R11 4.7K
R12 24K 2%
R13 20K 2%
C4 .10 16V
C7 .10 16V
C10 10 25V
C11 33 20V
C12 .01
C13 .01
C14 .01
C15 .01
C16 .01
C17 .01

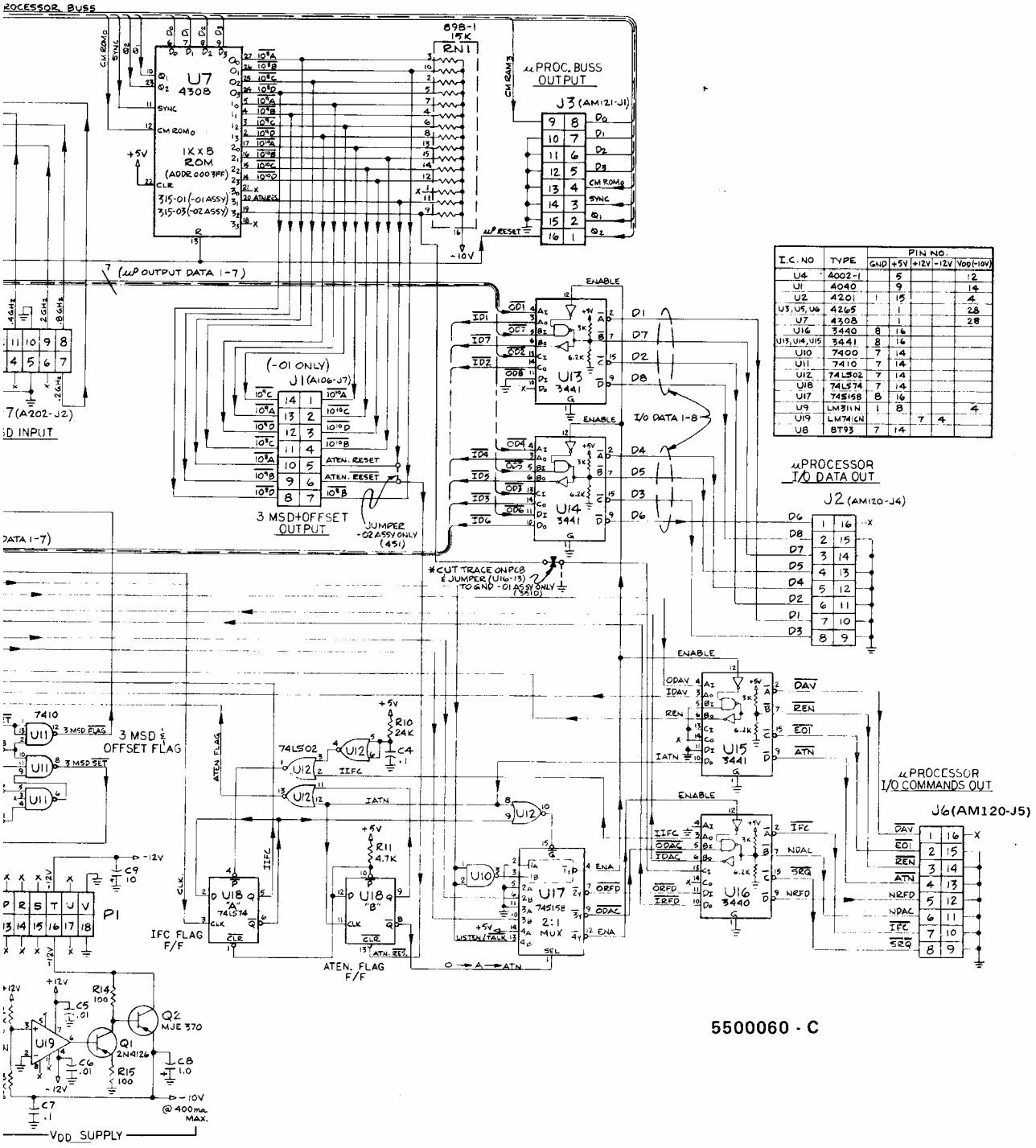


I.C. NO.	TYPE	PIN NO. GND	+5	+12	-12	Vbb(-9)
U1	4040		9			14
U2	4201	1	15			4
U3,5,6	4265		1			28
U7	4308		1			28
U8	8T93	7	14			
U9	LM311	1	8			4
U12	LS02	7	14			
U13-15	3441	8	16			
U16	3440	8	16			
U17	S158	8	16			
U18,21	LS74	7	14			
U19	LM741CN			7	4	
U10,20	7400	7	14			
U11	LS123	8	16			
U4	4002-1		5			12

REF DESIGNATION	
LAST USED	NOT USED
U21	
R19	
C20	
CR2	
Q2	
J6	J1
Y1	

Figure P5-9. GPIB Microprocessor Component Locator


MICROPROCESSOR BUSS
U5 4265
I/O PORTS MODE 6 (ADDR 80 H)
BCD INPUTS
μP RESET
U6 4265
I/O PORTS MODE 7 (ADDR 80 H)
U7 4308
1K X 8 ROM (ADDR 000-3FF)
315-01 (-01 ASSY)
315-03 (-02 ASSY)
(μP OUTPUT DATA 1-7)
BCD VALID
BCD A
BCD B
BCD C
BCD D
SR DATA
SR CLK.
μP INH.
J4 (AM120-J6)
U4 4002-1 (20X4X6 RAM)
3 MSD FLAG
(-01 ONLY) J7 (A202-J2)
3 MSD INPUT
U9 LM311N
(μP INPUT DATA 1-7)
U3 4265
I/O PORTS MODE 7 (ADDR 80 H)
MICRO-PROCESSOR
U1 4040
U2 4201
CLOCK & RESET
Y1 5.185 MHz
J5 (AM121-J5)
P1
7410
3 MSD FLAG RESET
3 MSD SET
3 MSD & OFFSET FLAG
ATEN. FLAG
IFC FLAG F/F
U18 74LS74
U19 LM741CN
Q1 2N4126
Q2 MJE 370
-10V @ 400ma MAX.
VDD SUPPLY



I.C. NO	TYPE	PIN NO. GND	+5V	+12V	-12V	VDD(-10V)
U4	4002-1		5			12
U1	4040		9			14
U2	4201	1	15			4
U3, U5, U6	4265		1			28
U7	4308		1			28
U16	3440	8	16			
U13, U14, U15	3441	8	16			
U10	7400	7	14			
U11	7410	7	14			
U12	74LS02	7	14			
U18	74LS74	7	14			
U17	745158	8	16			
U9	LM311N	1	8			4
U19	LM741CN			7	4	
U8	BT93	7	14			

Figure P5-10. GPIB Microprocessor Schematic

AM120
BCD OUTPUT
(2020086)

The BCD Output PC board (AM120) transfers 7 BCD inputs from the counter to the Microprocessor (μP) board (AM100) and, in the process, transforms the 7 inputs from 4-bit parallel data to 4-bit serial information. AM120 includes the Print/Inhibit logic, and the GPIB connector.

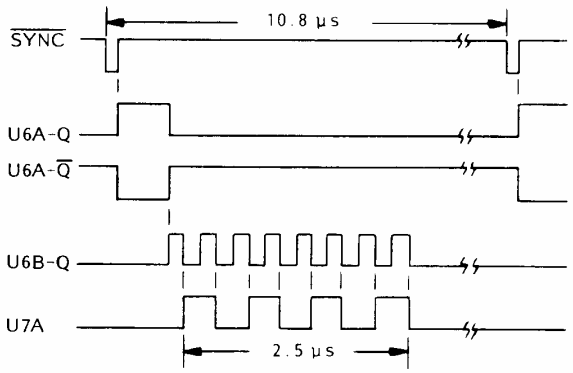
BCD information from Count Chain board A103 enters AM120 through J1 and J2, and connects to the inputs of four Shift registers (U1-U4).

CASCADED SHIFT REGISTERS

Shift Registers (U1-U4) are cascaded such that the serial output of one stage feeds the serial input of the next. The four output lines of U4 are fed through J6 to the μP. The most-significant-bit (MSB) of U4 (pin 10) is fed back to the serial input of U1 (pin 10). In this way, data can be circulated by the repeated application of the clock pulse from the Shift Register Timing Control. Data is loaded into the registers by a high to low transistion of the BCD Valid signal. Transformation of the BCD inputs from parallel to serial is accomplished by having the last four bits of data from U4 clocked by the Timing Control section and sent via J6 to the μP.

SHIFT REGISTER TIMING CONTROL

The Timing Control consists of U5C, U6, U7, and their associated components. Each time SYNC is active (high to low transistion), U6A will generate a pulse which resets decade counter U7. Clocking of U7 is accomplished by U8B which is configured as a free-running MV, with the Q output delayed by C7/R5 and fed back to the gate input (U6 pin 10). When clocked, U7 generates the four pulses used by the cascaded Shift Registers, after which U7 pin 11 turns off U6B at pin 9. (See Timing Diagram.)



PRINT/INHIBIT LOGIC

The Print/Inhibit logic consists of the U9 circuitry. When both the μInhibit signal from the μP, and the Print Command from the counter go high, BCD Valid is generated. This signal goes to the cascaded Shift Registers and loads the BCD data. The signal also goes to U9D, thus generating Inhibit and stopping the counter Sequence Generator in the Print Sequence.

The signal is also sent to the μP through J6, signaling that the BCD data from the counter has been loaded into the Shift Registers. When the μP acknowledges BCD Valid, it places μInhibit in the low state, and begins reading data from the Shift Registers.

YIG PRESET SHIFT REGISTER

U8 is a serial-in/parallel-out Shift Register under μP control, and is used to send the YIG Preset value to the counter (through J3).

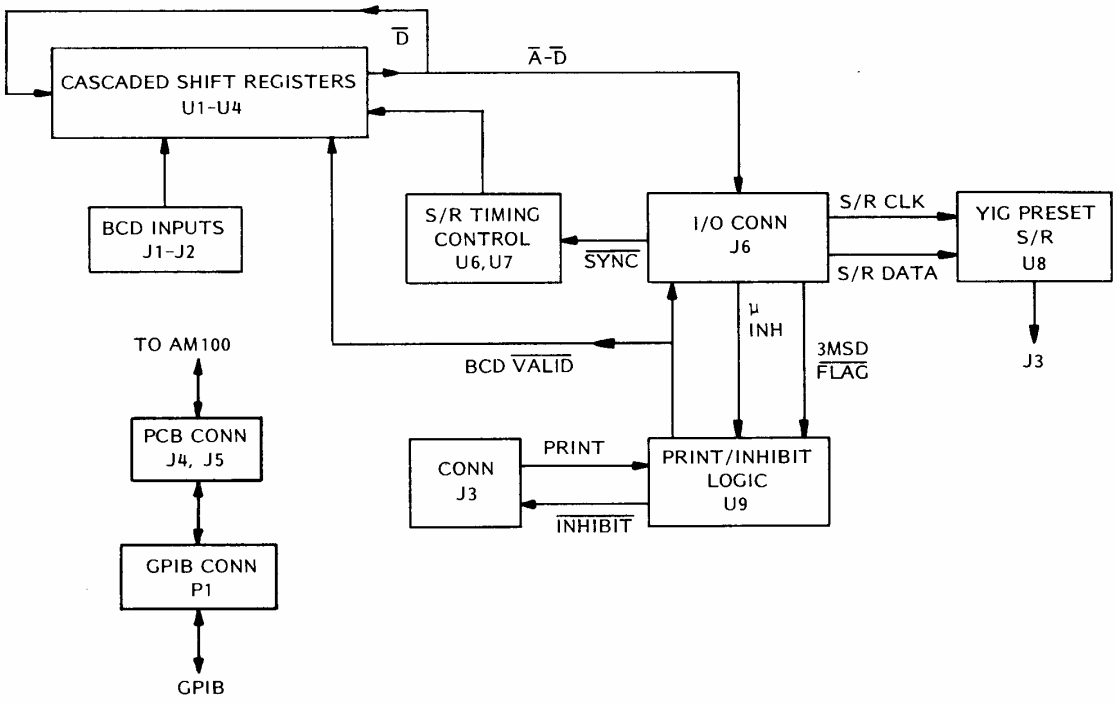


FIGURE P5-11. BCD OUTPUT DIAGRAM

AM 120 BCD OUTPUT, GPIB

2020086 - E

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
AM120	BCD Output, GPIB	2020086	1	EIP	34257
C1	Cer, .1μF, 20%, 16V	2150012	1	RT16 - 0.12	
C2	Cer, .01μF, 20%, 100V	2150003	3	TG - S10	56289
C3	C2				
C4	C2				
C5	Mica, 10pF, 5%, 500V	2250001	2	DM-15-100J	72136
C6	C5				
C7	Mica, 220pF, 5%, 500V	2250011	1	DM15-221J	72136
R1	Comp, 4.7K, 5%, 1/4 W	4010472	1	RC07GF472J	81349
R2	Comp, 10K, 5%, 1/4 W	4010103	1	RC07GF103J	81349
R3	Comp, 20K, 5%, 1/4 W	4010203	1	RC07GF203J	81349
R4	Comp, 2.2K, 5%, 1/4 W	4010222	1	RC07GF222J	81349
R5	Comp, 1K, 5%, 1/4 W	4010102	1	RC07GF102J	81349
U1	P/S IN/S Out, 8 Bit, SR	3070005	3	74L165P	01295
U2	U1				
U3	U1				
U4	4 Bit, Shift Register	3007495	1	7495N	27014
U5	Hex Inverter	3007404	1	7404N	27014
U6	TTL/MONOSTABLE MV	3070003	1	74L123P	28324
U7	Decade Counter	3007490	1	749ON	27014
U8	IN/P Out, 8 Bit Shift Reg	3070004	1	74L164P	01295
U9	Quad, 2INP, NAND Gate	3070010	1	74L00N	27014

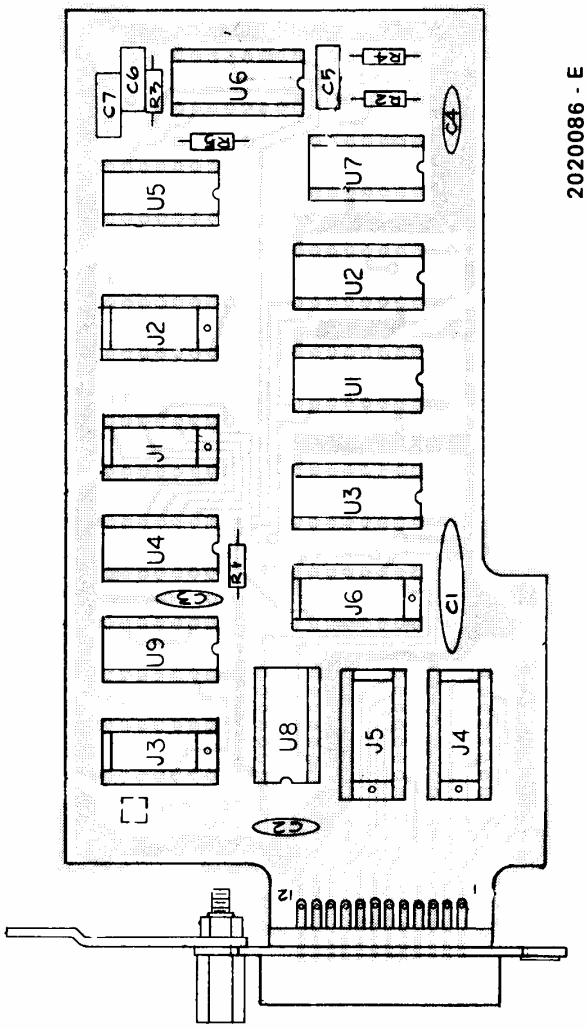
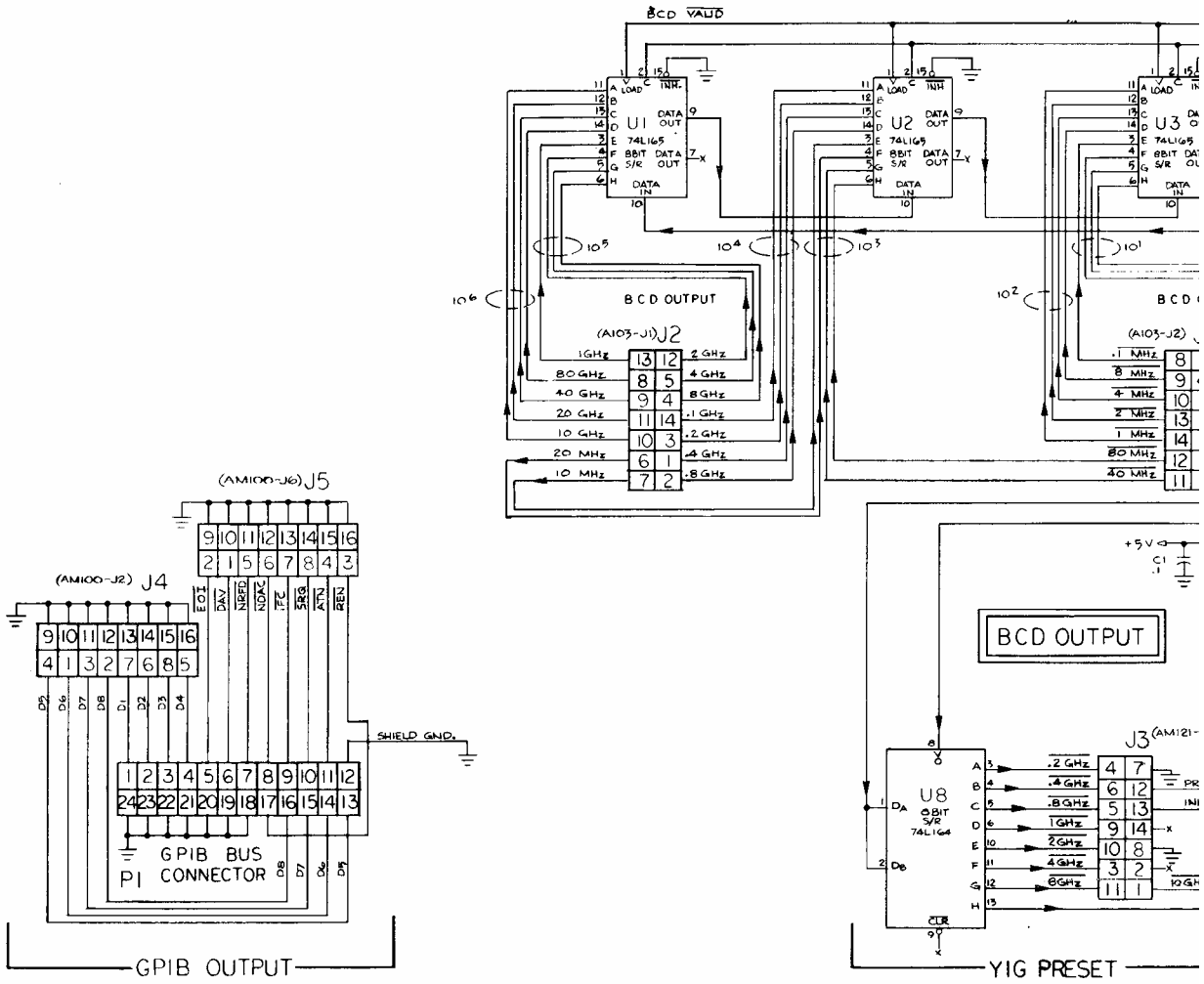


Figure P5-12. BCD Output Component Locator

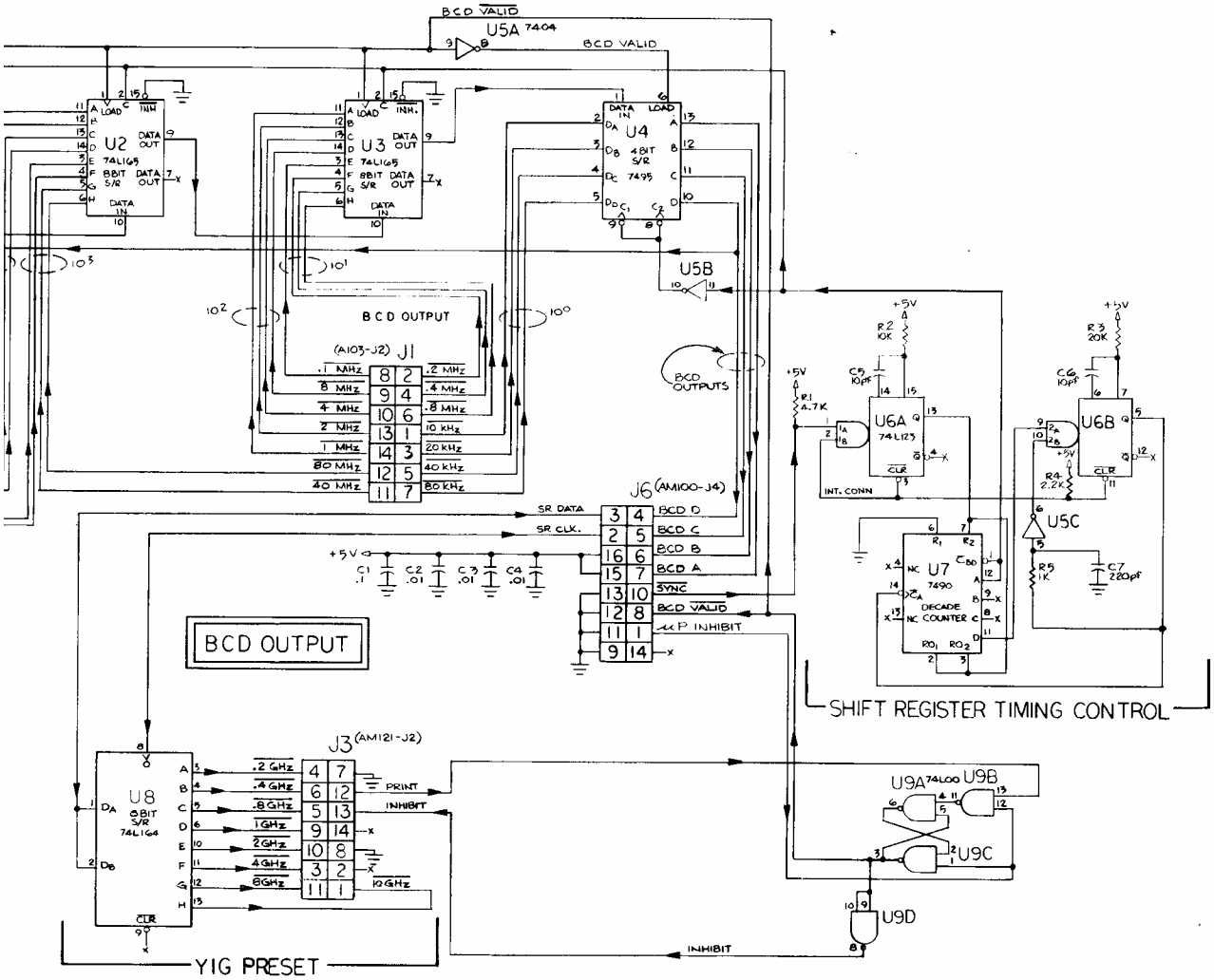


I.C. NO.	TYPE	PIN NO GND	PIN NO +5V
U3	7404 N	7	14
U7	7490 N	10	5
U4	7495 N	7	14
U9	74L00N	7	14
U6	74L123N	8	16
U8	74LI64 N	7	14
U1, U2, U3	74LI65 N	8	16

NOT USED

U6

LAST REF. DESIG.	NOT USED
C7	
R3	
U9	
J6	
P1	



5500086 - C

TYPE	PIN NO GND	+5V
7404 N	7	14
7490 N	10	5
7495 N	7	14
74L00N	7	14
74L123N	8	16
74LI64 N	7	14
74LI65N	8	16

NOT USED

U6

LAST REF. DESIG.	NOT USED
C7	
R5	
U9	
J6	
P1	

Figure P5-13. BCD Output Schematic

AM 121
REMOTE/LOCAL
(2020087)

The Remote/Local Control board provides the user with remote or local selection of counter front panel functions, and inputs data from the Address-Talk Mode switches.

PROCESSOR DATA BUS

J1 connects the Microprocessor (μP) control bus to U1. The signals are as follows:

01, 02	Non-overlapping clock signals which determine timing.
SYNC	Synchronization signal generated by the μP, indicates the beginning of a processor cycle.
$D_0 - D_3$	Bi-directional data bus. All address, instruction, and data communication between μP and system components are transferred on these lines.
CM-ROM_0	Chip enable for the ROM (U7). Generated by the μP.
PROC RESET	A negative level reset command which clears all output buffers of the support components (U1, U7 during power up.

NOTE: All above signals are at MOS levels.

1K x 8 ROM and 16 I/O PORTS

U1 is a read-only-memory (ROM), and contains the lower 1K of the 2K system program. (Address range: 400-7FF.) U1 communicates with the μP through the processor data bus in accordance with the 4040 system description. Associated with the ROM are 16 input/output lines. These lines are specified such that 12 are latching outputs and four are inputs. The 12 output lines ($0_0 - 2_3$ of U7) are MOS level, but are made TTL compatible by resistor network RN1.

The four MOS level lines designated as inputs ($3_0 - 3_3$ of U7) are used to sample the switch positions ($S_0 - S_3$) of the Address-Talk Mode switch (S1 - S7). ROM U7 has internal pull-down resistors, while the switches (S1 - S7) supply the +5 V level. The remaining signals from the Address-Talk switch (SW1, Test), go to the μP and are sampled there.

REMOTE/LOCAL CONTROL

U2 is a latch which stores the fact that REN has occurred and MLA was received. When these two conditions are met, $\overline{\text{RMT SET}}$ is pulsed low, and the counter receives its data from I/O ports located on U1. When the REN signal is cleared (low), the latch is disabled and the counter receives local program information through J2-4, J6-7.

2:1 MUX

U3 - U6 are 2:1 MUX's which, in the remote mode, transmit information from U1, and in the local mode, transmit information from J2-4, J6 and J7. These connectors are also used to send local/remote information to other parts of the counter.

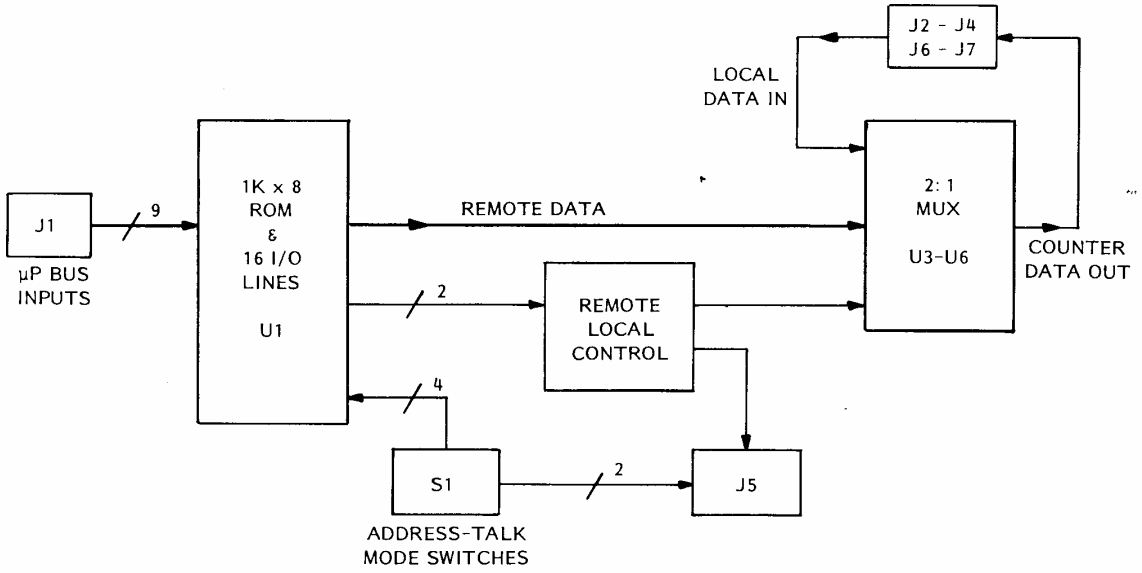
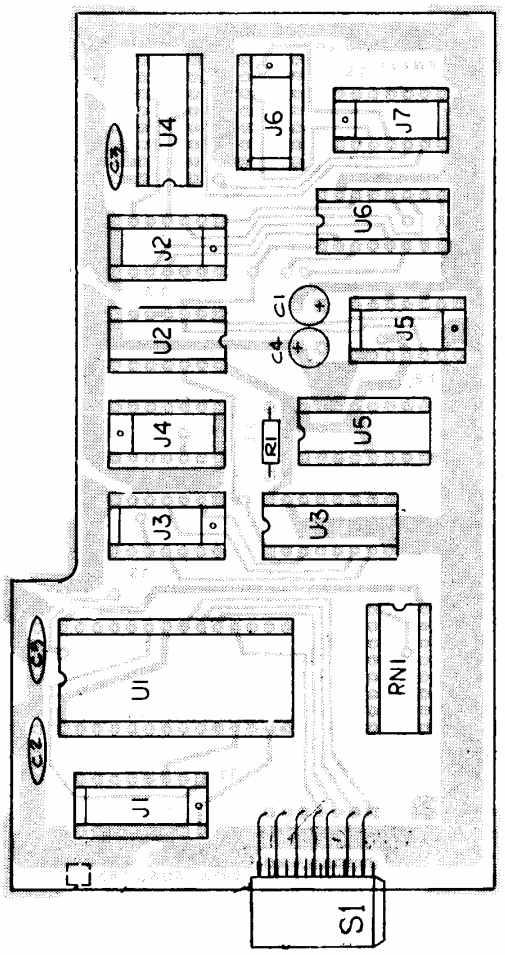


FIGURE P5-14. REMOTE/LOCAL DIAGRAM

AM121 REMOTE/LOCAL CONTROL

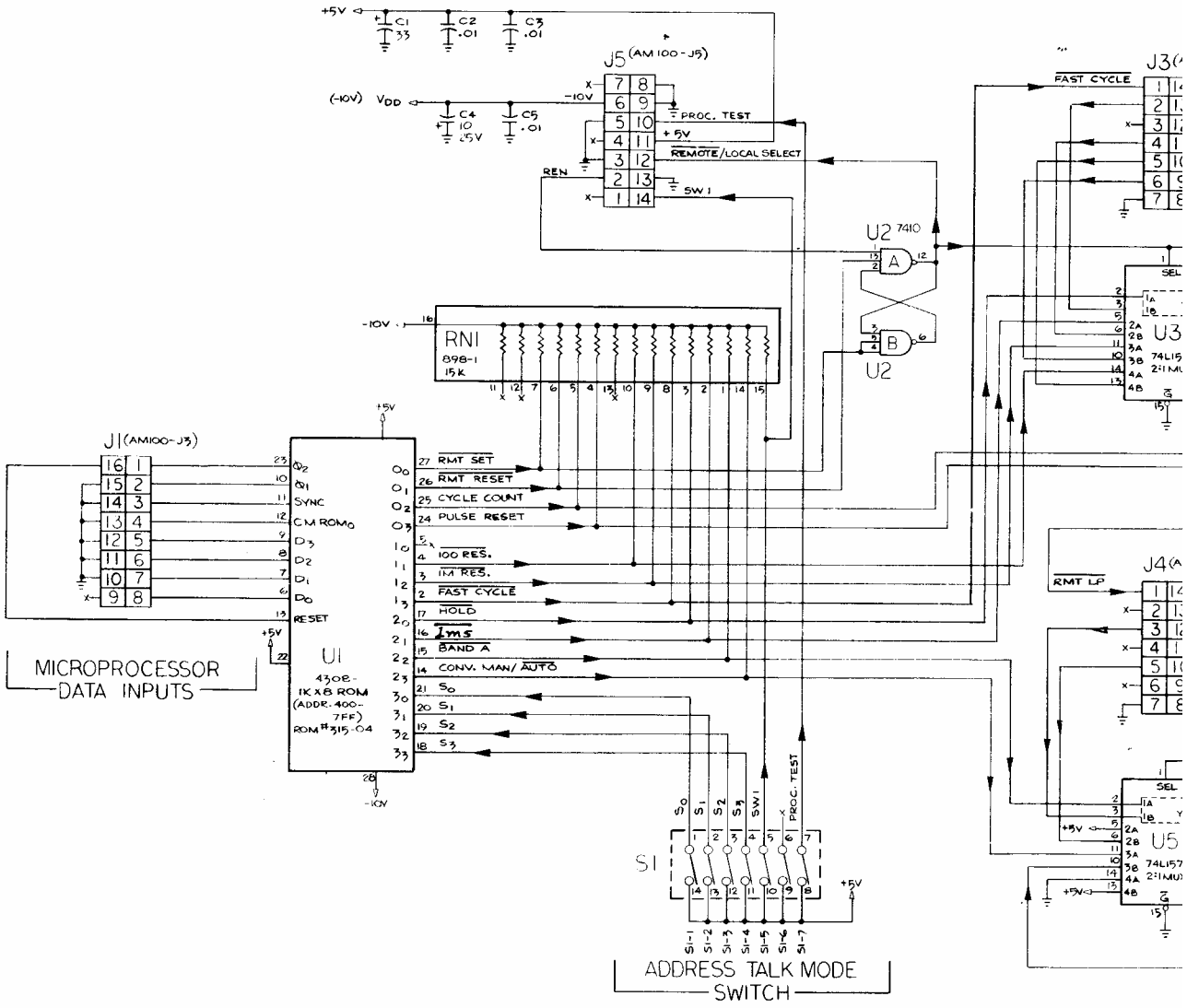
2020087 - E

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
AM121	Remote/Local Control	2020087	1	EIP	34257
C1	Tant, 33μF, 10%, 10V	2300015	1	TAG20 - 33/10	14433
C2	Cer, .01μF, 20%, 100V	2150003	3	TG - S10	56289
C3	C2				
C4	Tant, 10μF, 20%, 25V	2300029	1	TAPA10M25	14433
C5	C2				
R1	Comp, 150, 5%, 1/4 W	4010151	1	RC07GF151J	81349
RN1	Network, 15K	4170001	1	898-1-R15K	80740
S1	7 Position SPST, PGMT	4540003	1	1007-692	23880
U1	Rom, 4 Bit I/O	3150004	1	4308/3250	34649
U2	Tri, 3INP, NAND Gate	3007410	1	741ON	27014
U3	Quad, 2INP, MUX	3070003	4	74L157P	27014
U4 thru U6	U3				



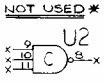
2020087 - E

Figure P5-15. Remote / Local Component Locator

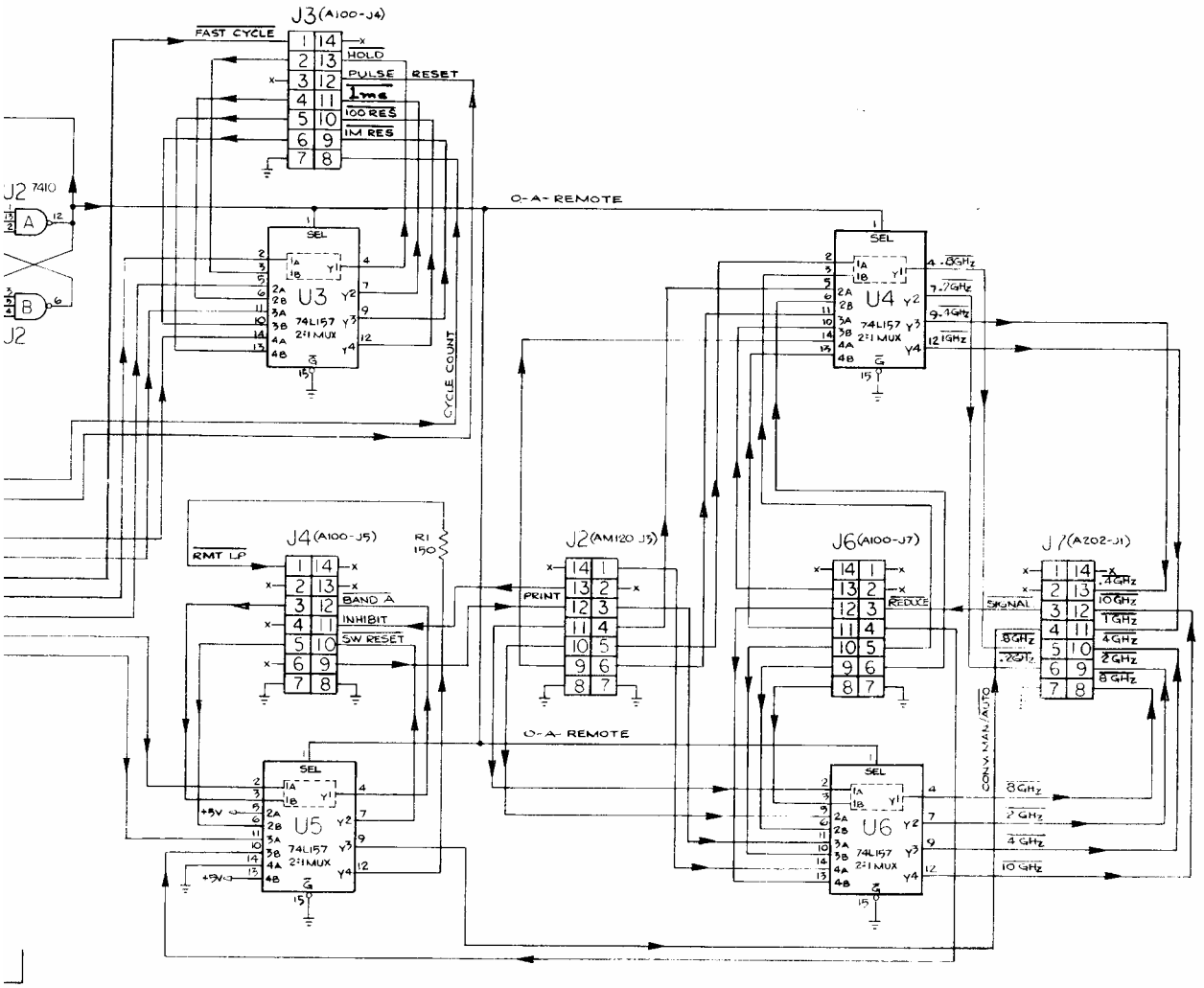


I.C. NO	TYPE	PIN NO.		
		GND	+5V	-10V
U1	4308-4	—	1	28
* U2	7410	7	14	—
U3, U4, U5, U6	74L157	8	16	—

NOT USED *



LAST DESIG.	NOT USED
C5	
R1	
RN1	
U6	
J7	



5500087 - B

LAST DESIG.	NOT USED
C5	
R1	
RN1	
U6	
J7	

Figure P5-16. Remote / Local (AM 121) Schematic

Appendix A
List of Manufacturers

FSCM	MANUFACTURER
0000X	Any Manufacturer of this product.
00656	Aerovox Inc., 740 Belleville Ave, New Bedford, MA 02741
00809	Croven Ltd., Whitby, Ontario, Canada
01121	Allen-Bradley Co., South Milwaukee, WI 53204
01295	Texas Instruments Inc., Dallas, TX 75222
02660	Amphenol Connector Div., Bunker Ramo Corp., Broadview, IL 60153
02735	Solid State Div. RCA Corp., Somerville, NJ 08876
04618	American Pamcor Inc., Paoli, PA 19301
04713	Motorola Inc., Semiconductor Div., Phoenix, AZ 85008
06665	Precision Monolithic Inc., 1500 Space Park Drive, Santa Clara, CA 95050
07263	Fairchild Semiconductor, Mountain View, CA 94040
08717	Sloan Company, Sun Valley, CA 91352
09353	C & K Components Inc., Watertown, MA 02172
11236	CTS of Berne Inc., Berne, IN 46711
11237	CTS, Keen, Paso Robles, CA 93446
12463	Optronics Mfg., 2420 S. 60th St., Omaha, NE 68106
14158	AVX, Filters, 10080 Willow Creek Rd., San Diego, CA 92131
14298	American Components Inc., Conshohocken, PA 19428
14433	ITT Semiconductor Div., West Palm Beach, FL 33401
14455	Quality Hardware Mfg. Co., 12605 Daphine, Hawthorn, CA 90250
14655	Cornell Dubilier, Dept. 150, Ave. L, Newark, NJ 07101
18324	Signetics Corp., Sunnyvale, CA 94086
23880	Stanford Applied Engineering Inc., Santa Clara, CA 95050
23036	Pamotor Inc., Burlingame, CA 94010
24546	Corning Glass Works, Bradford, PA 16701
26654	Varadyne Ind., Santa Monica, CA 90404
27014	National Semiconductor Corp., Santa Clara, CA 95051
28480	Hewlett-Packard Co., Palo Alto, CA 94304
29990	ATC Div., Phase Ind., Huntington Station, NY 11746
34257	EIP Microwave Inc., Santa Clara, CA 95134
34649	Intel Corp., 3585 SW 198th Ave., Aloha, OR 97005
51406	Murata Corp. of America, 1148 Franklin Rd., Marietta, GA 30068
56289	Sprague Electric Co., North Adams, MA 01247
59660	Tusonix Inc., 2155 Forbes Bldg., Tucson, AZ 85705
70903	Belden Corp., Chicago, IL 60644
71590	Centralab Div., Globe-Union Inc., Milwaukee, WI 53201
72136	Electro Motive Corp., Sub. of Int. Elect. Corp., Florence, Santa Clara, CA 95050
72259	Nytronics Inc., Pelham Manor, NY 10803
72982	Erie Technological Products Inc., Erie, PA 16512
73445	Amperex Electronic Corp., Hicksville, NY 11802
80031	Mepco/Electra Inc., Morristown, NJ 07960
80740	Beckman Instruments Inc., Fullerton, CA 92634
81349	Military Specification
86797	Rogan Bros. Inc., Skokie, IL 60076
91637	Dale Electronics Inc., Columbus, NE 68601
95275	Vitramon Inc., Bridgeport, CT 06601
98291	Sealectro, Mamaroneck, NY 10544
99800	Delavan Div. American Precision Industries, East Aurora, NY 14052